University of California, Berkeley
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Computer Science Division — EECS

Spring 2001 John Kubiatowicz

Homework Quiz (HW #5)

March 20, 2001
CS152 Computer Architecture and Engineering

This quiz covers one of the problems from homework #5.
Good Luck!

Your Name:	
SID Number:	
Discussion Section:	

Total:	

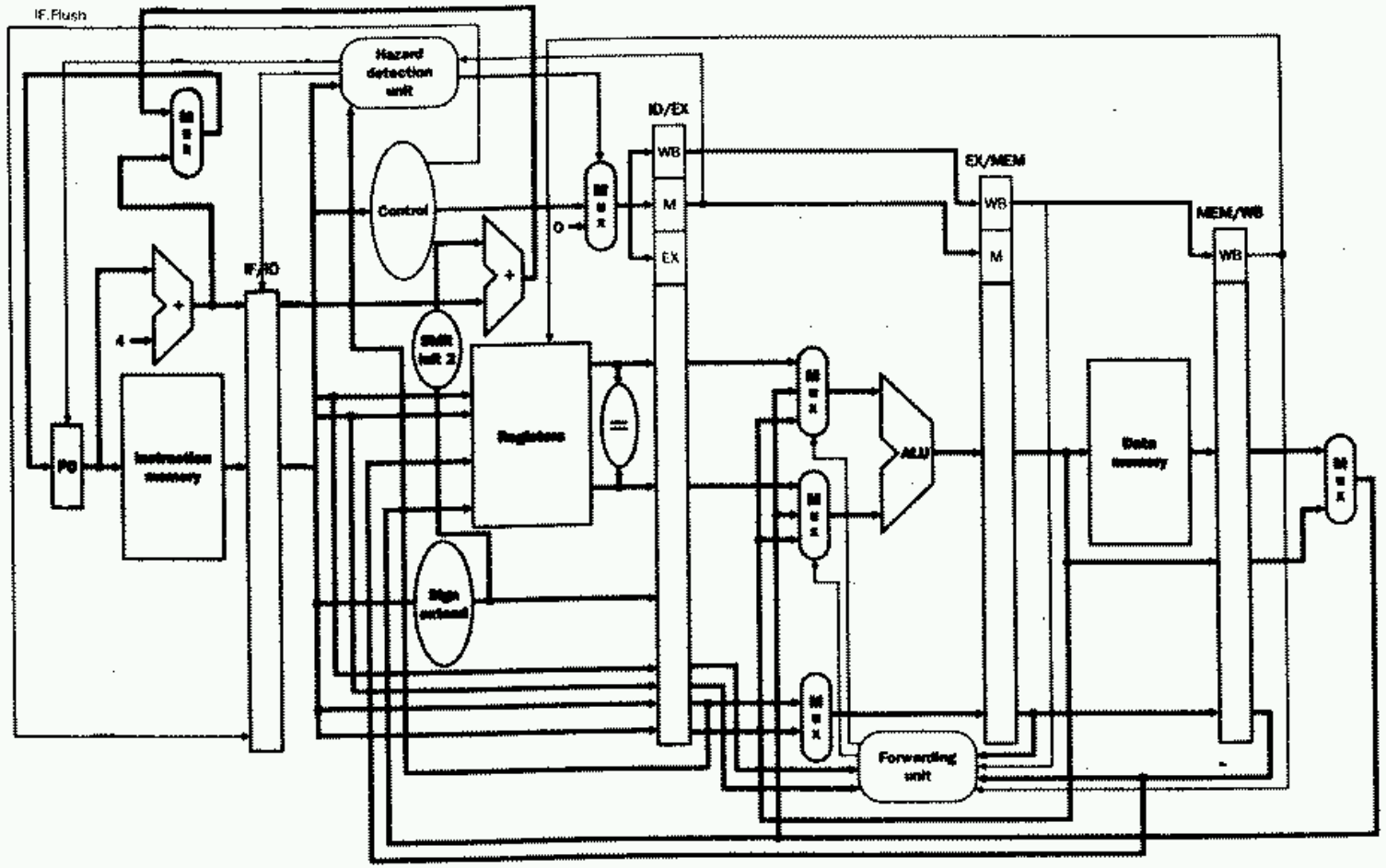

FIGURE 6.51 Datapath for branch, including hardware to flush the instruction that follows the branch. This optimization moves the branch decision from the fourth pipeline stage to the second; only one instruction that follows the branch will be in the pipe at that time. The control lines IF.Flush turns the fetched instruction into a nop by zeroing the IF/ID pipeline register. Although the flush line is shown coming from the control unit in this figure, in reality it comes from hardware that determines if a branch is taken, labeled with an equal sign to the right of the registers in the ID stage.

In problem 6.19 and 6.20, you explored hazards involving memory instructions. For your reference, Figure 6.51 from the book is reproduced on the previous page.

1. Consider the following instruction sequence (RAW hazard through memory):

```
sw  $2, 20($4)
lw  $5, 20($4)
```

   Does this require forwarding hardware *for maximum performa*nce? If yes, draw/describe the forwarding hardware and describe the control circuitry. If no, explain why not.

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2. Consider the following instruction sequence (RAW hazard through registers):

```
lw  $2, 20($4)
sw  $2, 100($5)
```

   Does this require forwarding hardware *for maximum performance*? If yes, draw/describe the forwarding hardware and describe the control circuitry. If no, explain why not.