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Computer Science Division — EECS

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Homework Quiz (HW #5)

October 27, 1999
CS152 Computer Architecture and Engineering

This quiz covers one of the problems from homework #5.
Good Luck!

Your Name:	
SID Number:	
Discussion Section:	

Total:	

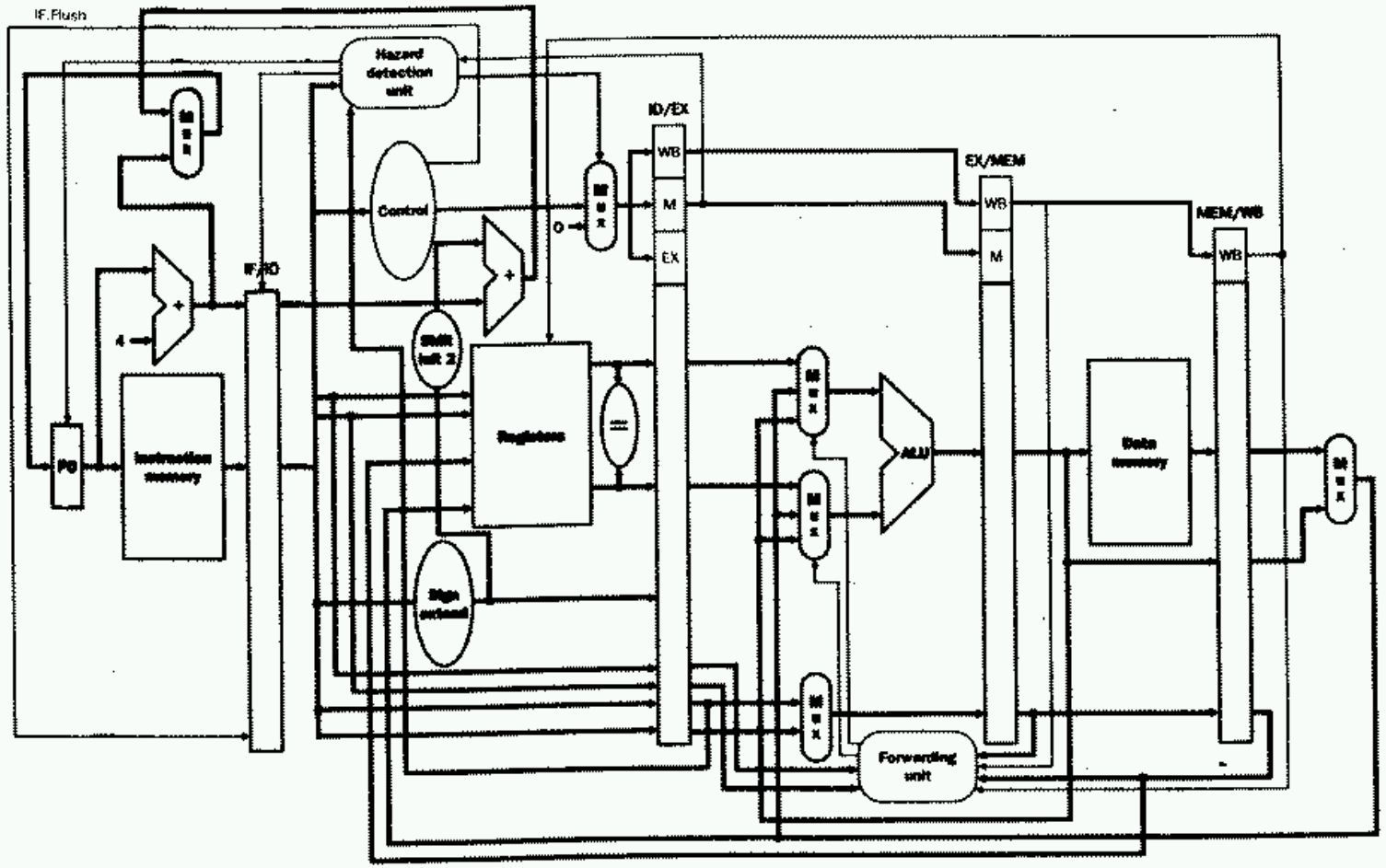

FIGURE 6.51 Datapath for branch, including hardware to flush the instruction that follows the branch. This optimization moves the branch decision from the fourth pipeline stage to the second; only one instruction that follows the branch will be in the pipe at that time. The control lines IF.Flush turns the fetched instruction into a nop by zeroing the IF/ID pipeline register. Although the flush line is shown coming from the control unit in this figure, in reality it comes from hardware that determines if a branch is taken, labeled with an equal sign to the right of the registers in the ID stage.

In problem 6.27, you were asked which stage branch decisions must be made to reduce the branch delay to a single cycle.

1. In which stage must branch decisions be made in order to support only one branch delay slot? Justify your answer.

2. Figure 6.51 from one of the printings of the book is reproduced on the previous page. Consider the following instruction sequence:

```
sub $2, $4, $5
beq $2, $3, somewhere
```

   Why doesn't this code sequence work properly on this hardware (this is a bug in the book!)?

3. Enhance the data path so that the code sequence of (2) works. Don't worry about control:

4. Suppose that the execute stage of the original hardware (figure 6.51) was the critical path (longest stage). What is the critical path after the modification for question #3 (be careful!)?