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Computer Science Division — EECS

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Homework Quiz (HW #6)

November 21, 2001
CS152 Computer Architecture and Engineering

This quiz combines two of the problems from homework #6.
Good Luck!

Your Name:	
SID Number:	
Discussion Section:	

Total:	

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Memory Heirarchy

This problem combines elements from chapter 7 and 8 problems. You have a 500 MHz processor with 2-levels of cache, 1 level of DRAM, and a DISK for virtual memory. Assume that it has a Harvard architecture (separate instruction and data cache at level 1). Assume that the memory system has the following parameters:

Component	Hit Time	Miss Rate	Block Size
First-Level Cache	1 cycle	4% Data 1% Instructions	64 bytes
Second-Level Cache	20 cycles + 1 cycle/64bits	2%	128 bytes
DRAM	100ns+ 25ns/8 bytes	1%	16K bytes
TLB	1 cycle	0.1%	16K bytes

Finally, assume that the TLB has a fill penalty of 40 cycles.

Question 1: Assume that the DRAM miss rate refers to a page fault. The DISK parameters are: Drive rotates at 12000RPM, transfer rate 32 MB/second, 10ms average seek time. What is the "Miss Penalty" for filling a DRAM page? You can treat MB=10^6 bytes and KB=10^3 bytes.

Miss penalty = seek time + rotational delay + transfer time

$$= 10\text{ms} + \frac{0.5 \cdot 60}{12000} + \frac{16x10^3}{32x10^6} = 13\text{ ms}$$

Question 2: Write an equation for $AMAT_{data}$ as seen by the processor. You do not have to generate an actual number. This equation should evaluate to a time in "ns", so make sure to check units. Hint: using a set of equations with symbolic values is probably the simplest thing to do.

$AMAT_{data}$=L1 hit time+L1 miss rate*(L2 hit time+L2 miss rate*(DRAM hit time+DRAM miss rate*DRAM miss penalty))
+ TLB miss rate*TLB miss penalty

=2ns + 0.04*(20cycles*2ns/cycle+128/8*2ns/cycle+0.01*(100ns+25ns/8bytes*16KB+0.001*13ms))+0.001*40ns

=30.16ns