University of California, Berkeley
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Computer Science Division — EECS

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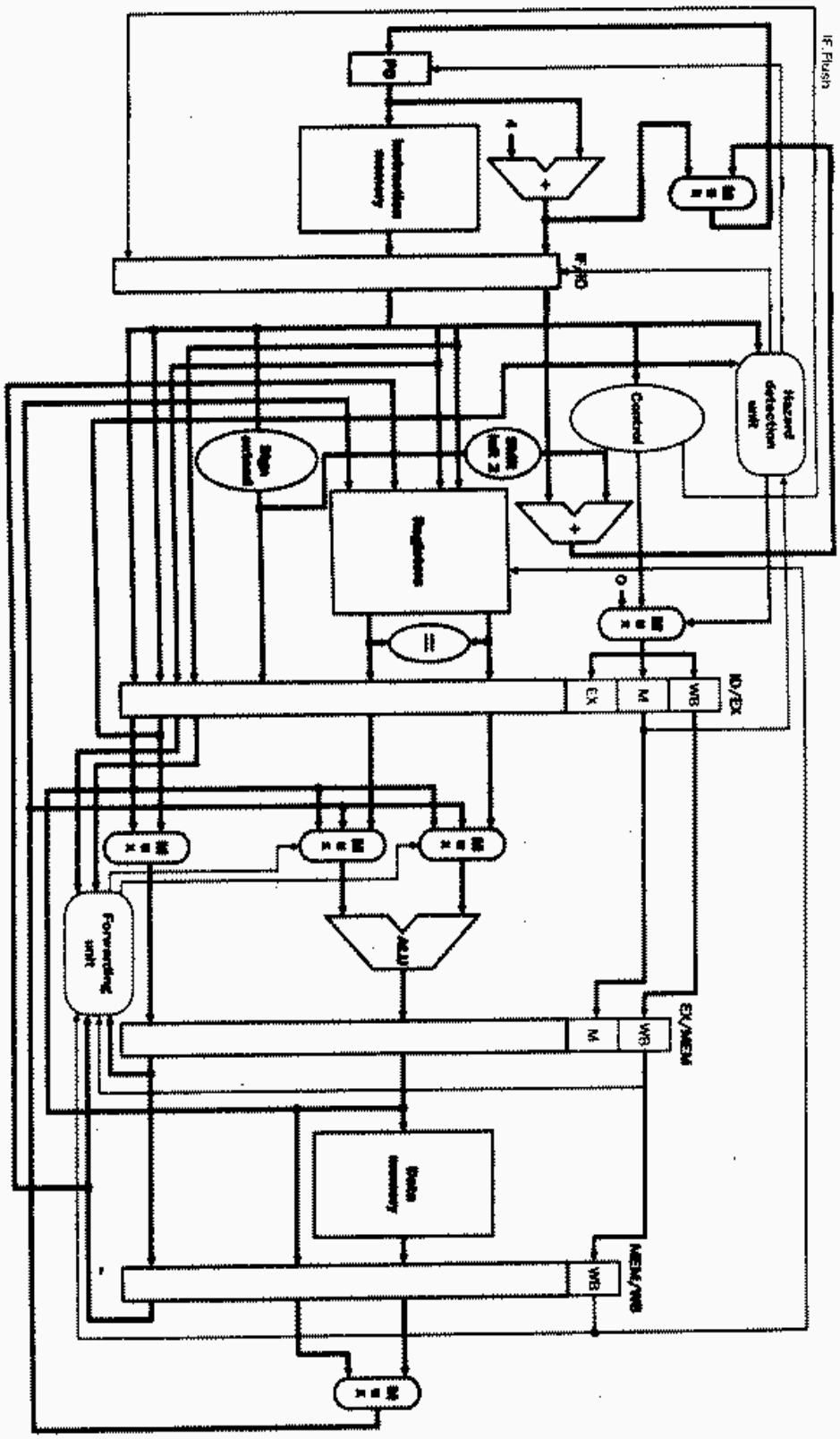
Homework Quiz (HW #5)

November 7, 2001
CS152 Computer Architecture and Engineering

This quiz covers one of the problems from homework #5.
Good Luck!

Your Name:	
SID Number:	
Discussion Section:	

Total:	


IF Flush
Hazard detection unit
Control
Registers
ID/EX
EX
M
WB
Forwarding unit
EX/MEM
MEM/WB

In problems 6.26 and 6.27, you were asked to consider a pipeline *which does not support a delayed branch*. Figure 6.51 from one of the printings of the book is reproduced on the previous page.

1. In this datapath, how many instructions must be "flushed" out of the pipeline when a branch is taken? Explain.

2. What must be in the "Control" oval in order to support flushing (i.e. when does it decide to assert IF.Flush)? What exactly does the "IF.Flush" signal do?

3. Consider the following instruction sequence:

```
sub $2, $4, $5
beq $2, $3, somewhere
```

   Why doesn't this code sequence work properly on this hardware (this is a bug in the book!)?

4. Can you fix this problem without adding hardware (i.e. only moving hardware around)? Explain. How many instructions must be "flushed" on a taken branch now?