This quiz covers one of the problems from homework #5.
Good Luck!

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In problem 6.27, you were asked which stage branch decisions must be made to reduce the branch delay to a single cycle.
1. In which stage must branch decisions be made in order to support only one branch delay slot? Justify your answer.

2. Figure 6.51 from one of the printings of the book is reproduced on the previous page. Consider the following instruction sequence:
   
   sub $2, $4, $5
   beq $2, $3, somewhere

   Why doesn’t this code sequence work properly on this hardware (this is a bug in the book?)?

3. Enhance the data path so that the code sequence of (2) works. Don’t worry about control:

4. Suppose that the execute stage of the original hardware (figure 6.51) was the critical path (longest stage). What is the critical path after the modification for question #3 (be careful!)?