This quiz covers one of the problems from homework #4.
Good Luck!

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The DoubleSwap instruction

Figure 1: A multicycle data path

Figure 1 shows the multicycle datapath from the book. In your homework, you implemented the \texttt{add3} instruction, which had four registers as operands. You were also asked to implement the \texttt{swap} instruction which swapped two registers. In this problem, you will implement the \texttt{doubleswap} instruction, which takes 4 registers and swaps pairs of values:

\begin{verbatim}
doubleswap $t1,$t2,$t3,$t4
\rightarrow \{t1 \leftrightarrow t2, t3 \leftrightarrow t4\}
\end{verbatim}

The coding of this instruction is as follows: $t1$ is in the RS field, $t2$ is in the RT field, $t3$ is in the RD field, and $t4$ is in the bottom 5 bits of the instruction (the FUNCT field).

\textbf{Problem 1a}: What changes are required to the data path in order to support this instruction? \textit{Note that you must not change the register file block itself; it should have 2 read ports and 1 write port.}
### Problem 1b:
Above, we show the microcode assembly-language and the microcode for 2 of the six instructions that we coded in class. What changes are needed to the microcode assembly language to support the **doubleswap** instruction?

### Problem 1c:
Write complete microcode for **doubleswap**, including the *fetch* and *dispatch* cycles. Be careful not to make changes that would interfere with the other instructions. What is the CPI of your new instruction?