Microprocessor Chip with Photonic I/O

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Abstract: In this work, we provide an overview of the technology and architecture of a microprocessor chip with optical I/O. Zero-change photonics integration enabled the chip to be fabricated in a commercial electronics CMOS foundry.

1. Introduction

While silicon photonics has established itself as a dense, low-cost replacement for discrete optics in networking applications, it has yet to reach an integration level necessary to drive a new generation of photonics-enabled computing devices and architectures. A key barrier to integration lies in the manufacturing process conflicts between CMOS devices and photonic devices [1], which often requires costly process development or unwieldy co-packaged modules to resolve, making the development of integrated photonics systems a lengthy and risky endeavor. To enable very large scale integration (VLSI) of on-chip photonics and electronics, our research team took an alternative approach. Instead of developing a process in which to fabricate our photonic devices, we took a commercial CMOS process as-is, followed all of its manufacturing rules, and overcame its constraints by way of innovation in device and system design. Through this approach, which we call the *zero-change* approach, we were able to demonstrate the world's first microprocessor with photonic I/O [2]. In this work, we discuss the architecture of the microprocessor chip and the evolution of the zero-change photonics platform on which it was realized.

2. Microprocessor chip architecture

The microprocessor chip, which we internally designated as *EOS22* (Fig. 1), contains a processor, a 1 MB memory bank, optical transceiver banks, and independent transceiver test sites. EOS22 featured two primary I/O interfaces. The first is the Host Target Interface (HTIF), a 16-bit wide full-duplex parallel electrical interface used for low-speed processor configuration and general purpose communication. The second interface is to memory, which is a full-duplex optical interface managed by the processor's memory controller and mimics the timings of a DDR-like DRAM memory bus. The processor itself is a dual-core RISC-V processor [3]. Each core contains RISC-V integer cores created via the *Rocket* chip generator [4] and is integrated with the *Hwacha* vector accelerator [5]. The 1MB memory bank is a block of SRAM organized into 8 independent banks, with interface logic emulating DRAM timings. For clocking, two on-chip phase-locked loops (PLLs) output clocks up to 2.5GHz for all on-chip components, synthesized from low-frequency clock inputs to the chip.

Both the processor and the 1 MB memory bank are each connected to an optical transmitter bank and an optical receiver bank. Each optical transmitter or receiver bank is an 11-λ DWDM macro utilizing microring-based modulators or receivers. On the transmit side, CW laser light of each λ from a fiber couples into the transmit bus waveguide through a vertical grating coupler (VGC), is modulated by a modulator microring, and couples into an output fiber through a second VGC. On the receive side, modulated light of each λ enters the receiver bank through an input VGC, is demuxed by a receive filter microring and dropped onto a photodetector.

To create an optical processor memory system, we setup two EOS22 chips (Fig. 2). We configure one chip in *processor mode*, where only the RISC-V processor cores and its transceiver banks are active, and the second chip in *memory mode*, where only the 1 MB memory bank and its associated transceiver banks are active. To execute a program, the program binary is first loaded via HTIF on the *processor mode* chip, which makes direct memory accesses (DMA) to write the program binary into the 1MB memory bank on the *memory mode* chip through the

optical memory interface. A reset command to the processor is then issued via HTIF and the program begins execution, accessing the optical memory interface as the processor fetches program instructions and manipulates program data. We note that while traditional DRAM interfaces are half-duplex, the optical memory interface of EOS22 is full-duplex, enabling simultaneous read data and write data transfer to and from memory.
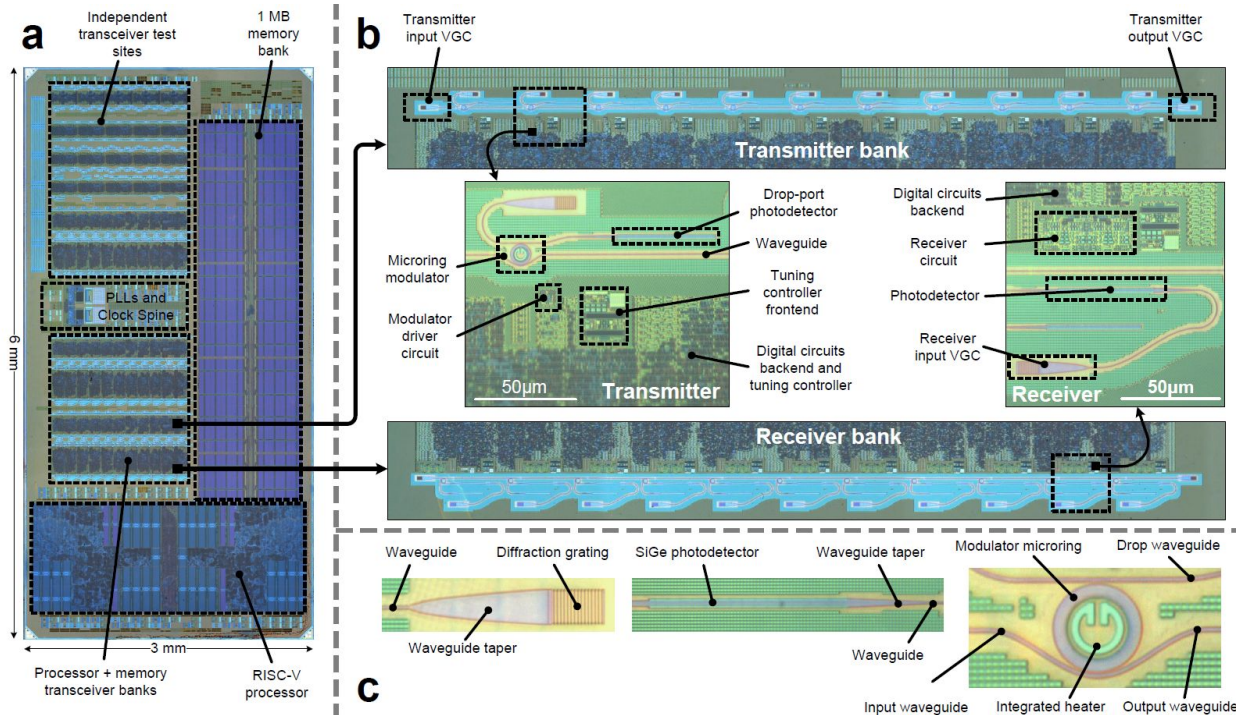

Fig. 1. Microprocessor chip (EOS22) die photo with main features labeled (a), zoom-ins of the microring-based transmitter and receiver banks (b), and micrographs of the grating coupler, SiGe photodetector, and spoked-ring cavity modulator devices (c).
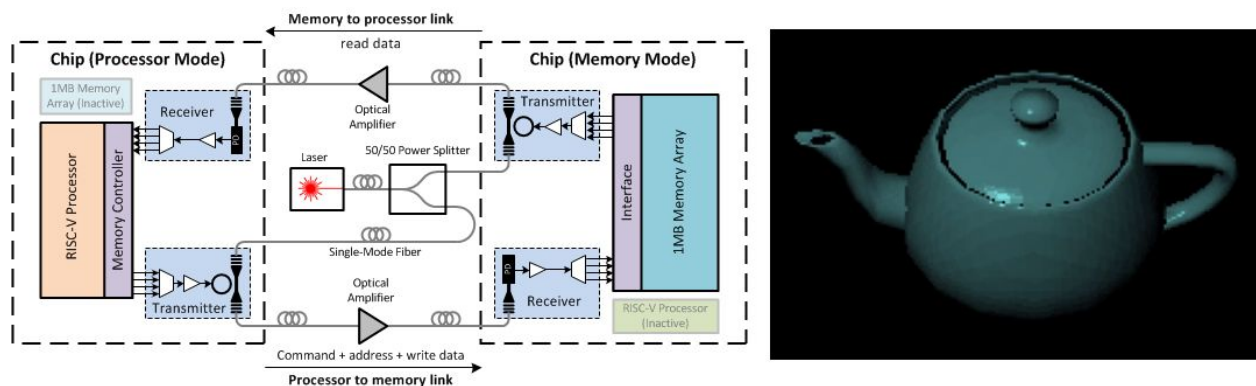

Fig. 2. Optical memory system using two EOS22 chips where one chip is in *processor mode* and the other in *memory mode* (left) and output of a teapot rendering program running on the program using the optical memory system

3. Optical devices and device evolution

The presence of only a single crystalline silicon (c-Si) layer thickness made the creation of active devices a challenge. First-generation resonant cavities utilized rib waveguides created using the polysilicon (poly-Si) on top of the c-Si [6, 7]. However, quality factors for these early devices were low due to the high loss of the poly-Si layer (>60dB/cm). Second generation resonators utilized a *spoked-ring* cavity design [8], which enabled low-loss device contacts to be made along the inner side wall of c-Si only rings and brought about the first carrier-depletion modulators on the platform (Fig. 3). While early spoked ring devices operated at 5Gbps NRZ, subsequent device bug fixes, junction geometry optimizations [9], and driver circuit improvements brought about >12.5Gbps NRZ and,

more recently, 20Gb/s NRZ and 40 Gb/s PAM4 transmitters on the platform [10]. Embedded microheaters enable efficient thermal tuning at an efficiency of 3.2μW/GHz (~10mW/FSR) and closed-loop thermal tuning by on-chip control circuits have been demonstrated with tuning ranges exceeding 500GHz (2.5nm) [11].
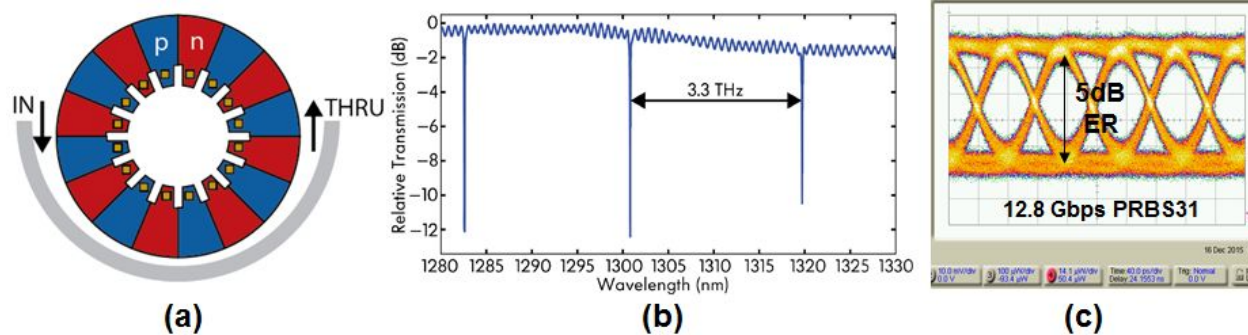

Fig. 3. (a) Spoked ring resonant cavity, (b) typical passive wavelength spectrum of a spoked ring modulator, and (c) 12.8Gbps NRZ transmit eye diagram with an on-chip $2V_{pp}$ modulator driver.

First-generation photodetectors were implemented in a linear rib-waveguide structure and limited to 0.023A/W, owing to the low mole fraction (weak absorption) of the process-native SiGe used for strain engineering PMOS transistors, and the need to use lossy poly-Si to create the rib-waveguide structure. We subsequently improved the photodetectors to 0.55A/W at 1180nm [12] by resonantly absorbing into the SiGe integrated into our spoked-ring cavity, simultaneously enhancing the effective absorption length of the SiGe through resonance and eliminating poly-Si in the design. This marked improvement in responsivity allowed us to shift the platform into the O-band (as opposed to the 1180nm band in the original work). A natively resonant photodetector also obviated the need for per-channel receive-side wavelength demux filters in the DWDM receiver bank. Finally, grating couplers have improved from 4-5dB fiber-to-chip coupling [2, 6], to 0.2dB in design and 0.5dB measured [13].

4. Conclusion

For silicon photonics to proliferate, it must adopt a path towards integration with CMOS. To be CMOS-integrated, we chose to design photonics in a commercial production CMOS SOI process and overcome the associated optical challenges through new device design, culminating in the demonstration of a microprocessor with optical I/O. Many of the initial limitations on the platform have also since been overcome.

5. References

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