A Comparison of Digital Droop Detection Techniques in ASAP7 FinFET

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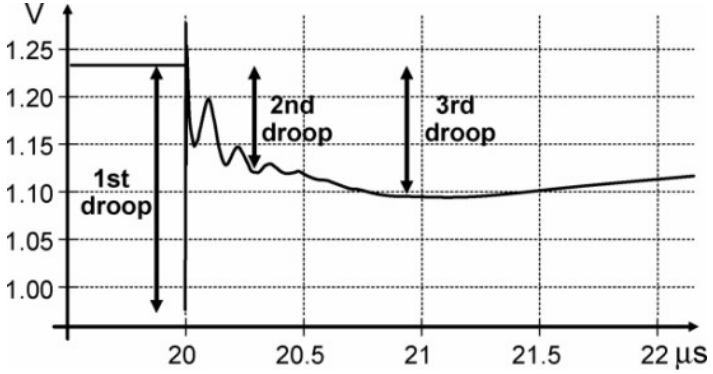
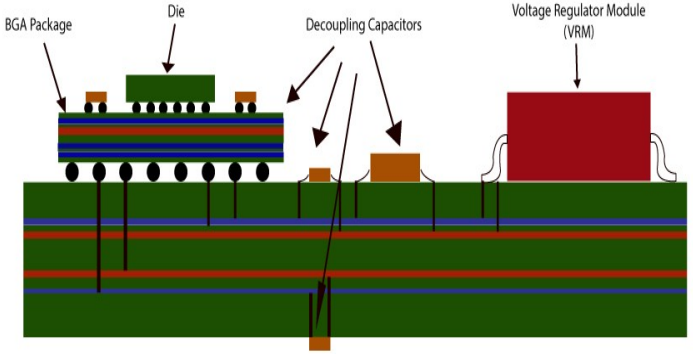
Outline

- Motivation
- Project topic and state of art
- NAND divider and ring oscillator droop detector, design methodology
- Design example and results in ASAP7
- Conclusion

The Need For Droop Detectors

- Power supply challenges of modern systems:
  - Scaling: more logic density, power consumption
  - Power gating: large current spikes
  - System and packaging limit achievable R's and L's
- Fast droop detectors required for system performance and reliability

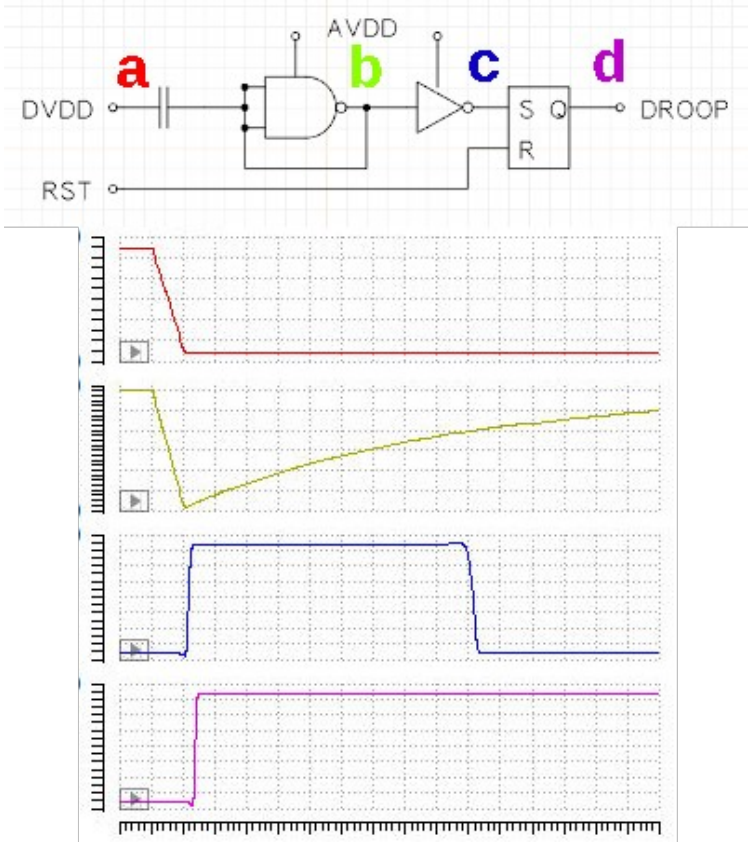




State Of Art

- Droop detector circuits: mixed-signal and fully-digital
- Part of overall system droop mitigation strategy
- Secondary treatment in existing literature
- Studied in isolation in separate process technologies
- **This work:** compare different fast single-cycle droop detectors in the same technology for the same design specifications

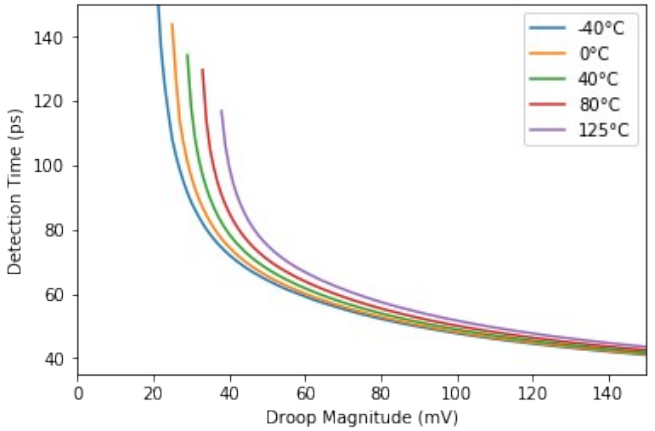
Droop Detection Technique: NAND Divider Detector

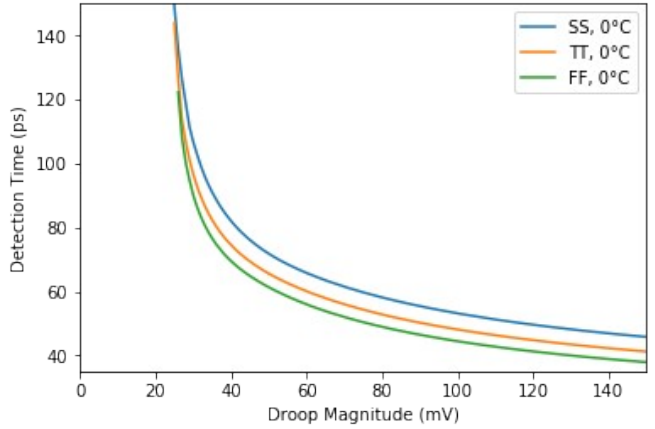


- Analog circuit in disguise
- Voltage divider (NAND gate) followed by comparator (inverter)
- Requires 2-terminal AC-coupling capacitor
- Requires separate, stable AVDD

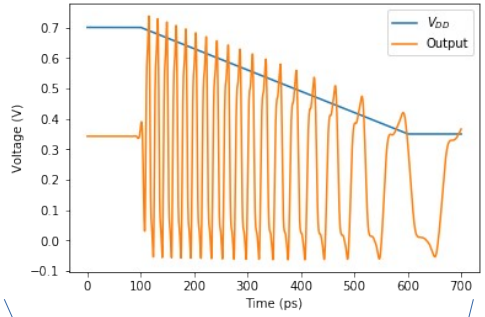
Design Methodology: NAND Divider Detector

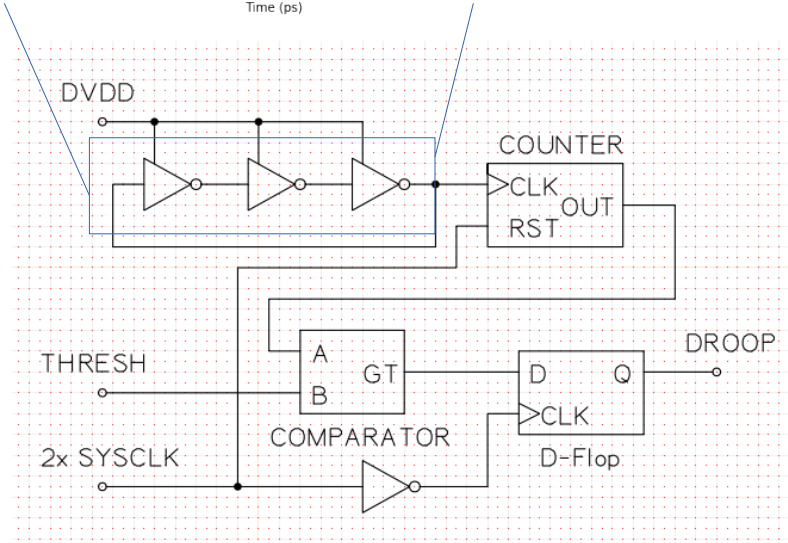
- Input high-pass network
  - C and W(INV) set input high-pass pole
  - Set low enough to capture the lowest droop frequency of interest
- Inverter chain
  - Minimize delay between high-pass node and latch
- Output latch
  - Any reasonable asynchronous latch





Droop Detection Technique: Ring Oscillator Detector

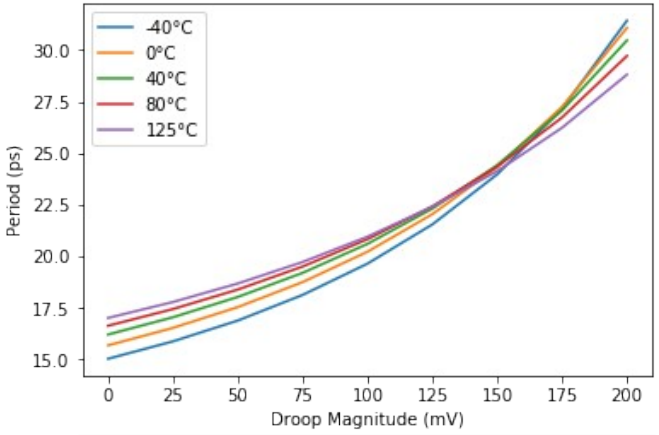


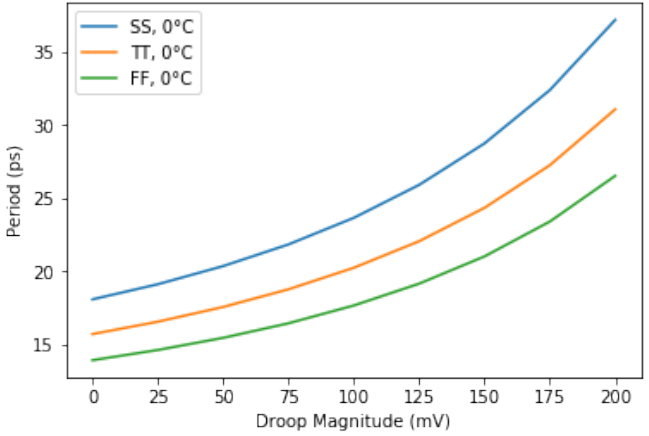


- Ring oscillator frequency changes instantaneously with VDD
- Use ring oscillator frequency as a measurement of voltage
- Frequency counter with programmable comparator threshold detects droops
- Fully synthesizable

Design Methodology: Ring Oscillator Detector

- Ring oscillator stages (N)
  - Pick N, simulate T_{min}
  - $\Delta T_{min} = T_{nom}^2 / T_{detection}$
- Counter threshold (M)
  - $M = T_{detection} / T_{nom}$
  - Account for worse-case corners





Design Examples in ASAP7

- Fast Design Example
  - Hypothetical high-performance desktop or server processor
  - Maximum boost frequency of 4 GHz
  - Half period: 125 ps
- Slow Design Example
  - Hypothetical low-power embedded or mobile processor
  - Core frequency of 800 MHz
  - Half period: 625 ps

Results

- NAND divider detector
  - Performs nearly 3x better in all measured metrics
  - Not fully synthesizable
- Chosen design metrics penalize ring oscillator detector for its process variability

Design Metric	NAND Divider	Ring Oscillator
Min. Detectable Droop (mV)	**38**	106
Temp. Sensitivity (uV/K)	**110**	360 / 450
Proc. Sensitivity (mV)	**2**	7.4 / 1.9
Fully Synthesizable	No	**Yes**

Conclusions

- Topology should be chosen according to specifications and design space exploration
- Design methodologies and automated generators help!
- For *these* specifications in ASAP7, NAND detector wins on performance

Questions?

References

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