A Comparison of Digital Droop Detection Techniques in ASAP7 FinFET

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The Need For Droop Detectors

- Power supply challenges of modern systems:
  - Scaling: more logic density, power consumption
  - Power gating: large current spikes
  - System and packaging limit achievable R’s and L’s

- Fast droop detectors required for system performance and reliability
Droop detector circuits: mixed-signal and fully-digital
Part of overall system droop mitigation strategy
Secondary treatment in existing literature
Studied in isolation in separate process technologies

This work: compare different fast single-cycle droop detectors in the same technology for the same design specifications
Droop Detection Technique: NAND Divider Detector

- Analog circuit in disguise
- Voltage divider (NAND gate) followed by comparator (inverter)
- Requires 2-terminal AC-coupling capacitor
- Requires separate, stable AVDD
Design Methodology: NAND Divider Detector

- Input high-pass network
  - C and W(INV) set input high-pass pole
  - Set low enough to capture the lowest droop frequency of interest

- Inverter chain
  - Minimize delay between high-pass node and latch

- Output latch
  - Any reasonable asynchronous latch
Droop Detection Technique: Ring Oscillator Detector

- Ring oscillator frequency changes instantaneously with VDD
- Use ring oscillator frequency as a measurement of voltage
- Frequency counter with programmable comparator threshold detects droops
- Fully synthesizable
Design Methodology: Ring Oscillator Detector

- Ring oscillator stages (N)
  - Pick N, simulate $T_{\text{min}}$
  - $\Delta T_{\text{min}} = \frac{T_{\text{nom}}^2}{T_{\text{detection}}}$

- Counter threshold (M)
  - $M = \frac{T_{\text{detection}}}{T_{\text{nom}}}$
  - Account for worse-case corners
Design Examples in ASAP7

- Fast Design Example
  - Hypothetical high-performance desktop or server processor
  - Maximum boost frequency of 4 GHz
  - Half period: 125 ps

- Slow Design Example
  - Hypothetical low-power embedded or mobile processor
  - Core frequency of 800 MHz
  - Half period: 625 ps
Results

• NAND divider detector
  - Performs nearly 3x better in all measured metrics
  - Not fully synthesizable
• Chosen design metrics penalize ring oscillator detector for its process variability

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<th>Design Metric</th>
<th>NAND Divider</th>
<th>Ring Oscillator</th>
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<tr>
<td>Min. Detectable Droop (mV)</td>
<td>38</td>
<td>106</td>
</tr>
<tr>
<td>Temp. Sensitivity (uV/K)</td>
<td>110</td>
<td>360 / 450</td>
</tr>
<tr>
<td>Proc. Sensitivity (mV)</td>
<td>2</td>
<td>7.4 / 1.9</td>
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<td>Fully Synthesizable</td>
<td>No</td>
<td>Yes</td>
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Conclusions

- Topology should be chosen according to specifications and design space exploration
- Design methodologies and automated generators help!
- For these specifications in ASAP7, NAND detector wins on performance
Questions?
References


- [7] X. Sun et. al, "A Combined All-Digital PLL-Buck Slack Regulation System with Autonomous CCM/DCM Transition Control and 82% Average Voltage-Margin Reduction in a 0.6-to-1.0V Cortex-M0 Processor," ISSCC 2018.
