EE244 Project Proposal: Process Aware Timing Analysis

Wojtek Poppe ,Zheng Guo, and Chung-Hsun Lin
EECS Department, U. C. Berkeley

Good points: Title slide – we know who is doing the project!!!

Motivation

- Process variations have a significant effect on the circuit performance and yield. This problem will only get worse in the future technology generations.
- Statistical distribution of transistor threshold voltages do not capture enough processing details.
- Random threshold voltage variations is not well characterized.
- There is big gap between circuit designers and processing engineers.

Good points: Timely, not project dependent

Weaknesses in other projects: Tied to specific projects not general industry/technology trends

Problem Definition

- How to effectively communicate processing knowledge to circuit designers
  - Aerial simulator can predict CD distribution based on layout
  - Significant amounts of variations can be predicted by moving within the your process window
- How to use processing knowledge to design more robust circuits with minimum trade-off
  - Identify problem areas with aerial image and circuit simulation
  - Discriminately apply robust circuit techniques locally
- Identify what portion of random threshold voltage variation can be attributed to predictable systematic CD variation

A little general, needs to be focused further

Literature Survey

- **Jie Yang, Capodieci L, Sylvester D. Advanced timing analysis based on post-OPC extraction of critical dimensions. IEEE. 2005, pp.359-64. Piscataway, NJ, USA**
  - **This paper defines an aerial image simulator to static timing analyzer flow that we are going to use in our project.**
- **Orshansky M, Milor L, Pinhong Chen, Keutzer K, Chenming Hu. Impact of spatial intrachip gate length variability on the performance of high-speed digital circuits., vol.21, no.5, May 2002, pp.544-53. Publisher: IEEE, USA.**
  - **One of the first papers to propose looking at transistors in a statistical fashion based on emperical Lgate data.**
- **Borkar S. Circuit techniques for subthreshold leakage avoidance, control and tolerance. IEEE. 2005, pp.421-4. Piscataway, NJ, USA.**
- **Friedberg P, Cao Y, Cain J, Wang R, Rabaey J, Spanos C. Modeling within-die spatial correlation effects for process-design co-optimization. Proceedings. 6th International Symposium on Quality Electronic Design. IEEE Comput. Soc. 2005, pp.516-21. Los Alamitos, CA, USA.**
  - **Paul used emperical data from Jason Cain's thesis that characterized intrachip, intra wafer, and inter wafer CD variation.**

These papers' statistics are skewed as CD data is extracted from perfect gratings which do not appear on actual chip layouts. The paper finds mostly systematic CD variation, which should be addressed by processing engineers since it is mostly layout/proximity independent. Designers should address CD variation effects that can be mitigated by changes in the design.

Good points: real bibliography, explains relevance of papers, also course professor is referenced – always a good idea ☺

Literature Survey

- J. A. G. Jess, K. Kalafala, S. R. Naidu, R. H. J. M. Otten, and C. Visweswariah. Statistical timing for parametric yield prediction of digital integrated circuits. Design Automation Conference (DAC), Anaheim, CA, pages 932--937, June 2003.
  - Nice approach for statistical timing analysis based on Einstimer's static timer. However, like most work on statistical timing, it doest not provide a good link between processing and actual circuit implementation.
- C. Visweswariah, K. Ravindran, K. Kalafala, S. G. Walker, and S. Narayan. First-order incremental block-based statistical timing analysis. Design Automation Conference (DAC), San Diego, CA, pages 331--336, June 2004.
- Velenis, D.; Sundaresha, R.; Friedman, E.G. Buffer sizing for delay uncertainty induced by process variations. Electronics, Circuits and Systems, 2004. ICECS 2004. Proceedings of the 2004 11th IEEE International Conference on 13-15 Dec. 2004 Page(s):415 – 418
  - May be helpful for robust circuit techniques.
- Agarwal, A.; Blaauw, D.; Zolotov, V.;" Statistical timing analysis for intra-die process variations with spatial correlations,"Computer Aided Design, 2003. ICCAD-2003. International Conference on 9-13 Nov. 2003 Page(s):900 - 907
  - Nice reference for new statistical timing analysis algorithm.
- Yu Cao; Clark, L.T.; "Mapping statistical process variations toward circuit performance variability: an analytical modeling approach," Design Automation Conference, 2005. Proceedings. 42nd 13-17 June 2005 Page(s):658 – 663
  - Using analytical model to calculate the impact of process variation on the delay. Nice for comparison.
- Venkatraman, V.; Burleson, W.;"Impact of process variations on multi-level signaling for on-chip interconnects," VLSI Design, 2005. 18th International Conference on 2005 Page(s):362 - 367

Proposed Approach

- Automate aerial image simulation to take GDS file and output list of gate CDs (Mentor Graphics Calibre Workbench)
- Link aerial image simulation to HSPICE
- Build delay look-up table reference by processing conditions (dose and focus) within process window (HSPICE)
- Static timing analysis using look-up table (Primetime?)
- Evaluate novel robust circuit design techniques
- Extra Credits: investigate circuits for project validation

A little general, needs to be focused further

Timeline

- Week 1-3: Infrastructure, research of robust circuit techniques
- Week 3-6: build separate simulation modules
- Week 7-9: link modules together and evaluate robust circuit design techniques

Problem Definition- Loo, Wang

- SpaceWire is a general purpose interconnection network for spacecrafts.
- Given RTL verilog for SpaceWire's CODEC (i.e. its transmitter and receiver modules) the following specifications need to be verified:
  - Parity bit errors, credit errors, empty packets, escape errors, and data link disconnects must be detected
  - Upon error detection, the CODEC must stop current operations and enter reset state.
  - After a reset, CODEC must follow an "exchange of silence" protocol to resynchronize and restart data connection.
- We will manually abstract the verilog code and verify it with high-level model checking tools, such as SMV or SPIN.
- From this case study, we will attempt to develop an automated abstraction strategy for communication protocols.

Good points: very clear what problem is

Proposed Approach – Catanzaro, Sun, Toh

- Develop 3 applications on 3 different development environments comparing approaches based on metrics of:
  - Performance
  - Opacity – Abstraction of Architecture
  - Visibility – Freedom to Optimize for Architecture
  - Verification / Debugging

Good points: approach is clear

Timeline

Good points: when is very clear – add who as well

Major Dates:

- October 19 – Finish literature survey and finalize the details of our approach
- November 2 - Finish first round of simulations and successfully (we hope) perform DPA
- November 21 – Complete final simulations, compare results
- December 5 – Final project presentation ready

<table>
<tr><th colspan="2">October</th><th colspan="2">November</th><th>December</th></tr>
<tr><td colspan="2">Finish lit. survey
10/5 1019</td><td colspan="3"></td></tr>
<tr><td></td><td colspan="2">Implement Baseline and Duplicate AES/RNG
10/12 11/2</td><td colspan="2"></td></tr>
<tr><td colspan="2"></td><td>Perform DPA
10/19 11/2</td><td>Attack Our Design Make Comparisons
11/2 11/21</td><td></td></tr>
<tr><td colspan="3">Document and organize for final paper</td><td>Final Touches Due: 12/5</td><td></td></tr>
</table>