EECS 244: Introduction to CAD and the Course

Prof. Kurt Keutzer
EECS
keutzer@eecs.berkeley.edu
Lecture Overview

- Introduction to Kurt, Sanjit, .... and others
- Education and your future career
- CAD, Semiconductors and the broader economy
- Brief overview of CAD
- Goals of course
Skills you Will Need

- Wherever you go, after you graduate you will find yourself in a complex environment requiring knowledge and mastery over a variety of fields
  - In the good old days:
    - Ph. D’s join a university (e.g. Berkeley) or company (e.g. IBM) for life
    - Work locally in a single geographic area within an ethnically homogeneous group for entire career
    - Business concerns handled by “management”
    - Engineers left to focus on purely technical problems
    - Technical problems narrowly focused - coding theory, queuing theory, analog circuit design etc.

- New era
  - Moving around companies, universities, and geographies is the norm
  - Professors and engineers must create a “business case” for their research which lays out a plan for impact on business (i.e. revenue) or defense
  - Professor or engineer you need to be a complete corporation of size one with marketing and sales as well as engineering
  - Technical problems complex and interdisciplinary. A system-on-a-chip is precisely that. A complex mix of HW, SW, user interface supporting a variety of applications

I hope you come to view this as an exciting opportunity. Your careers can be incomparably more interesting and satisfying than those of prior generations.
Educational process evolves relatively slowly
EECS curriculum still principally focused on science and engineering
Fortunately, the campus is diverse
Specifically:
- Engineering:
  - EECS curriculum focused on this and does a good to great job
- Marketing:
  - Strategic: Need to understand the broader economy, the value chain, and the key trends
  - Tactical: Need to understand customer needs and how to meet them
  - Need to understand how to merge these two – identify the right customer and meet their needs
  - Berkeley Management of Technology (MOT) program good at this
- Sales:
  - Need to communicate value to the end customer
  - Need to learn how to “close” the customer to get your ideas funded
  - Not sure how you’re going to learn this but excellent communication skills is a good start
- Today we’re going to a mini-course on marketing and CAD – warning – it may be the oddest first lecture you’ve ever had!!

How do we get these skills?
Introduction to Kurt

- Professor in EECS
- B. S. in mathematics from Maharishi International University 1978
- M. S. and Ph.D. in CS from Indiana University 1984
- AT&T Bell Labs, Area 11 1984-1991
- Developed a number of successful (internally) tools for hardware developers
- Plaid – Programmable Logic AID – used to create racks of switching system hardware
- DAGON – worked with Chuck Stroud and Mark Vancura to create a logic synthesis system for Bell Labs – dozens of IC’s developed with the system
Introduction to Kurt

- Synopsys, Inc. 1991-1998 (now 14th largest software company)
  - From Member of Research Staff of $30M 200 person company to SVP/CTO of $600M 3000 person company in 7 years
  - As CTO
  - Oversaw and reviewed technology of over 25 software products accounting for $600M in revenue
  - Identified new technology and market opportunities
  - Initiated and participated in a dozen corporate acquisitions
  - As Manager=>Director=>VP=>SVP or research
    - Initiated a number of product ideas and two complete products:
      - FPGA Express – FPGA synthesis software – brought to “product roll-out”
      - Formality – market leader in formal verification of circuits –

UC Berkeley 1998-present
- Professor of EECS
  - As teacher – EECS 244 (Intro to CAD), CS169 (Software Engineering)
  - Associate Director – Gigascale Systems Research Center 1998-2001
  - As a research advisor
    - MESCAL: modern embedded systems, compilers, architectures, and languages – 8 students
Introduction to Kurt

As an entrepreneur:
- Everest Design (acquired SNPS, 1999) – investor/TAB
- Right Track CAD (acquired by Altera, 2000) – angel investor/TAB
- Everest Design (acquired SNPS, 1999) – investor/TAB
- Right Track CAD (acquired by Altera, 2000) – angel investor/TAB
- Everest Design (acquired SNPS, 1999) – investor/TAB
- Right Track CAD (acquired by Altera, 2000) – angel investor/TAB

As a consultant:
- Ammocore, C-Cube Microsystems (IPO), CoWare, Hier Design
- CommandCad – Angel investor – founded 2004 – DFM start-up
- CommandCad – Angel investor – founded 2004 – DFM start-up
- CommandCad – Angel investor – founded 2004 – DFM start-up
- CommandCad – Angel investor – founded 2004 – DFM start-up
- CommandCad – Angel investor – founded 2004 – DFM start-up
- CommandCad – Angel investor – founded 2004 – DFM start-up
Lecture Overview

- Introduction to Kurt, Sanjit, .... and others
- Education and your future career
- CAD, Semiconductors and the broader economy
- Brief overview of CAD
- Goals of course
The World and Electronic Systems

- The world is increasingly dependent on electronic systems
- The “first world” is entirely dependent on electronic systems
Electronic systems are entirely dependent on semiconductor components

- Electronic systems $1$ trillion
- Semiconductor industry $160$ ($141, 147?)$ billion

Electronic Industry Interdependence

**WW Electronic System Sales**

- 2000: $972B (-14%)
- 2001: $837B (-6%)
- 2002: $790B

**Semiconductor Market**

- 2000: $204.4B (-32%)
- 2001: $139.0B (1%)
- 2002: $140.5B

**Semi Equipment Market**

- 2000: $52.5B (-38%)
- 2001: $32.8B (-25%)
- 2002: $23.5B

**Semi Materials Market**

- 2000: $26.6B (-24%)
- 2001: $20.2B (7%)
- 2002: $21.6B

*Source: IC Insights, SEMI*
An Overview of the Markets

By Revenue (TTM)

- Services: 22%
- Financial: 15%
- Energy: 11%
- Healthcare: 5%
- Technology: 9%
- Transportation: 2%
- Basic Materials: 5%
- Capital Goods: 4%
- Utilities: 6%
- Consumer Cyclical: 11%
- Consumer/Non-Cyclical: 6%
- Conglomerates: 4%
- Entire Technology Sector: $1290B

12
Looking into the Technology Sector

**Entire Technology Sector**
$1290B

**Semi Industry**
$147B

**TTM Revenue Breakdown**

- **Software & Programming, 127,737**
- **Sci & Tech Instr, 31,610**
- **Office Eqpt, 49,305**
- **Electronic Instr. & Controls, 144,429**
- **Computer Storage Devices, 27,023**
- **Computer Services, 192,348**
- **Computer Hardware, 201,226**
- **Computer Networks, 15,805**
- **Comm Eqpt, 226,929**
- **Computer Peripherals, 126,283**
Where does the $141B go?

2002 Semiconductor Revenue by Application

Source: IDC

Scovel, 2003, Needham & Co.
Where does the $141B come from?

Scovel, 2003, Needham & Co.
Where does CAD fit in?

Electronic Systems

Silicon Foundries

Computer-aided Design

Real World

Integrated Circuit
Where does CAD fit in? Everywhere?

Real World

Electronic Systems

Semiconductor Industry

Silicon Foundries

Designer using CAD

Speech processing
Signal processing
Performance analysis

System modeling and synthesis

Formal verification
Logic synthesis
Place and route
Circuit simulation

Device simulation
Process modeling
Where does CAD fit in? The tools

Real World

Electronic Systems

Semiconductor Industry

Silicon Foundries

Matlab
Labview

SystemC
Metropolis
Ptolemy

Design compiler
Physical compiler
Apollo

BSIM
Spice
Pisces

Designer using CAD
Where does IC CAD fit in, specifically?

- Computer-aided design (CAD)/Electronic design automation (EDA) enables electronic systems
- CAD principally focuses on support for IC design:
  - ASIC and custom-oriented design flows
    - ASIC - 5% of Semi, $7B – e.g. Automatic Target Recognition ASIC in a military system
    - Microprocessors, DSPs, and ASSP - 43%, $60B – e.g. PowerPC, TI TMS320C54, Intel IXP2800
  - Human intensive custom design flows
    - Portions of high performance microprocessors – e.g. Pentium 3
    - FPGA, PLD – 2% of Semi, $3B – e.g. Xilinx 2VP50
  - Human intensive analog design flows
    - Analog ICs – 14% of Semi, $19B
    - Memories – 20% of Semi, $28B
  - Value of CAD to end designer (i.e. customer) depends on the degree to which it significantly eases and automates the design process
  - Revenue of CAD depends on value, size of market served, and buying behavior
- Small portion of CAD industry supports board-level design
Software Market Segmentation

Software Market (not incl services)
$100.9B

Software & Services Market
$229.8B
## Largest Software Companies - 8/2003

<table>
<thead>
<tr>
<th>Corporation</th>
<th>Ticker</th>
<th>Market</th>
<th>Rev</th>
<th>Marg</th>
<th>P/E</th>
<th>Price</th>
<th>High</th>
<th>Low</th>
</tr>
</thead>
<tbody>
<tr>
<td>14. Synopsys, Inc</td>
<td>SNPS</td>
<td>$5051</td>
<td>$1106</td>
<td>(16.2)</td>
<td>NM</td>
<td>$65.0</td>
<td>$65.5</td>
<td>$31.8</td>
</tr>
<tr>
<td>15. Amdocs Ltd</td>
<td>DOX</td>
<td>$4598</td>
<td>$1427</td>
<td>8.1</td>
<td>40.3</td>
<td>$21.3</td>
<td>$27.3</td>
<td>$5.85</td>
</tr>
<tr>
<td>16. Siebel</td>
<td>SEBL</td>
<td>$4595</td>
<td>$1418</td>
<td>(8.2)</td>
<td>NM</td>
<td>$9.30</td>
<td>$12.2</td>
<td>$5.33</td>
</tr>
<tr>
<td>17. Check Point Software</td>
<td>CHKP</td>
<td>$3974</td>
<td>$425</td>
<td>58.2</td>
<td>16.6</td>
<td>$16.2</td>
<td>$22.2</td>
<td>$12.6</td>
</tr>
<tr>
<td>18. Cadence Design</td>
<td>CDN</td>
<td>$3543</td>
<td>$1136</td>
<td>6.2</td>
<td>50.8</td>
<td>$13.0</td>
<td>$15.6</td>
<td>$8.65</td>
</tr>
<tr>
<td>19. Mercury Interactive</td>
<td>MERQ</td>
<td>$3398</td>
<td>$444</td>
<td>15.1</td>
<td>52.7</td>
<td>$39.8</td>
<td>$45.6</td>
<td>$15.2</td>
</tr>
<tr>
<td>20. Verisign</td>
<td>VRSN</td>
<td>$3307</td>
<td>$1112</td>
<td>(28.4)</td>
<td>NM</td>
<td>$13.9</td>
<td>$16.1</td>
<td>$3.92</td>
</tr>
</tbody>
</table>
Electronic systems and semiconductor components are entirely dependent on computer-aided design/electronic design automation tools

- Electronic systems $1 trillion
- Semiconductor industry $160B ($141, 147B?)
- EDA industry $3B

Sources: Gartner Group/Dataquest, Rose Associates; January, 2000
http://www.facsnet.org/tools/sci_tech/tech/biz/
- This is a snapshot – it’s important to understand the trends
The Inverted Pyramid

World economy > $33 Trillion

Electronic systems > $1 Trillion

Semiconductor > $141B

CAD $4B
Gross Domestic Product vs ES vs Semi

http://www.icknowledge.com/economics/growth_rate.html
What are the trends?

- World economic trends: 4-5% growth rate?
- Electronic system trends: Overall 7% growth rate
- Semiconductor trends: Cyclical semiconductor revenue, overall a 15-16% cumulative growth rate
- Results in electronic systems becoming an increasing portion of world revenue
- Results in semiconductors becoming an increasing portion of electronics systems
- In other words, the world is spending more of their money on electronic systems (e.g. cell phones and playstations) and an increasing amount of the $$ you pay for a Playstation goes to the semiconductor components
Increasing Semiconductor Content in E Systems

Electronic System Semiconductor Content

Source: ST, TI, IC Insights

*Forecast
Dramatic Increase in Design Costs

- Going forward, the total cost of design is rising more than 100% per process generation

Source: Handel Jones
IBS Inc.
Changing ASIC/ASSP Economics

- Optimistically, ASIC/ASSP revenues growing 10 – 15 % year

  - Engineering portion of budget is supposed to be trimmed every year (but never is)
  - Total chip development costs rising 30 – 100% year
  - Implies fewer IC designs (doing more applications) - every process generation going forward!!
  - Fewer IC design starts means less EDA revenue going forward
Total IC Designs

Handel Jones, IBS
9/23/2002
**EDA Industry Trends**

**Projected**

G. Smith, Chief EDA Analyst Gartner Dataquest, June 2005

- Increase in revenue based on “Electronic System Level (ESL) design
Review of Trends

- World economic trends: World GDP ~3% growth rate
- Electronic system trends: Overall 7% growth rate
- Semiconductor trends: Cyclical semiconductor revenue, overall a 15-16% cumulative growth rate
- Results in electronic systems becoming an increasing portion of world revenue
- Results in semiconductors becoming an increasing portion of electronics systems
- In other words, the world is spending more of their money on electronic systems (e.g. cell phones and playstations) and an increasing amount of the $$ you pay for a Playstation goes to the semiconductor components
- But ... CAD linked to design \textit{starts} and design \textit{seats} – fewer ASIC design starts means declining revenue
Lecture Overview

- Introduction to Kurt, Sanjit, .... and others
- Education and your future career
- CAD, Semiconductors and the broader economy
- Brief overview of CAD
- Goals of course
Driving CAD: Moore’s Law

Transistors

Microprocessors

10x/6 years
Clock Speed GHz.

- On-chip, global clock, high performance
- On-chip, local clock, high-performance
Role of CAD: Helping humans cope

Transistors vs. Intelligence Quotient

- Processor Complexity
- Avg. Human IQ
How does Moore’s Law drive CAD?

- Because the capability of integrated circuit technology scales so rapidly, traditionally we have had:
  - Exponentially more devices every process generation
  - Exponential increases in speed every process generation
- Will these trends continue?

- After a few process generations we need to do something fundamentally different
- CAD is not a field you can relax in!
Evolution of IC Design

McKinsey S-Curve

Results
(Design Productivity)


Transistor entry
Schematic Entry
RTL Synthesis

What’s next?
Evolution of the EDA Industry

Results
(Design Productivity)

- 1978: Transistor entry - Calma, Computervision
- 1985: Transistor entry - Calma, Computervision
- 1992: Schematic Entry - Daisy, Mentor, Valid
- 1999: Synthesis - Cadence, Synopsys

What’s next?

McKinsey S-Curve

Effort
(EDA tools effort)
**Transistor Era**

- **Key tools:**
  - Transistor-level layout – e.g. Calma workstation
  - Transistor-level simulation – e.g. Spice
  - Bonus: transistor-level compaction – e.g. Cabbage

- **Size of circuits:** 10’s of transistors to few thousand

- **Key abstractions and technologies:**
  - Transistor-level modeling, simulation
  - Logical gates- NAND, NOR, FF and cell libraries
  - Layout compaction
Gate-level Schematic Era

- **Key tools:**
  - gate-level layout editor – Daisy, Mentor, valid workstation
  - Gate-level simulator
  - Automated place and route

- **Size of circuits:** 3,000 – 35,000 gates (12,000 to 140,000 transistors)

- **Key abstractions and technologies:**
  - Logic-level simulation
  - Cell-based place and route
  - Static-timing analysis
Gate level models

- Border between transistor domain (analog) and digital domain
- Digital gate level models introduced to speed up digital simulation.
- Gate level model contains:
  - Logic behavior
  - Delays depending on: operating conditions, process, loading, signal slew rates
  - Setup and hold timing violation checks
- Gate level model parameters extracted from transistor level simulations and characterization of real gates.

J. Christiansen,
CERN - EP/MIC
Jorgen.Christiansen@cern.ch
RTL Synthesis Era

- **Key tools:**
  - Hardware-description language simulator – Verilog, VHDL
  - Logic synthesis tool - Synopsys
  - Automated place and route – Cadence, Avant!, Magma
- **Size of circuits:** 35,000 gates to ...?
- **Key abstractions and technologies:**
  - HDL simulation
  - Logic synthesis
  - Cell-based place and route
  - Static-timing analysis
  - Automatic-test pattern generation

```verilog
module Half_adder (Sum, C_out, A, B);
    output Sum, C_out;
    input A, B;
    xor M1 (Sum, A, B);
    and M2 (C_out, A, B);
endmodule

module Full_Adder (sum, c_out, a, b, c_in);
    output sum, c_out;
    input a, b, c_in;
    wire w1, w2, w3;
    Half_adder M1 (w1, w2, a, b);
    Half_adder M2 (sum, w3, w2, c_in);
    or M3 (c_out, w2, w3);
endmodule

module Full_Adder_4 (sum, c_out, a, b, c_in);
    output [3:0] sum;
    output c_out;
    input [3:0] a, b;
    input c_in;
    wire c_in2, c_in3, c_in4;
    Full_adder M1 (sum[0], c_in2, a[0], b[0], c_in);
    Full_adder M2 (sum[1], c_in3, a[1], b[1], c_in2);
    Full_adder M3 (sum[2], c_in4, a[2], b[2], c_in3);
    Full_adder M4 (sum[3], c_out, a[3], b[3], c_in4);
endmodule
```
module Half_adder (Sum, C_out, A, B);
  output Sum, C_out;
  input A, B;
  xor M1 (Sum, A, B);
  and M2 (C_out, A, B);
endmodule

module Full_Adder (sum, c_out, a, b, c_in);
  output sum, c_out;
  input a, b, c_in;
  wire w1, w2, w3;
  Half_adder M1 (w1, w2, a, b);
  Half_adder M2 (sum, w3, w2, c_in);
  or M3 (c_out, w2, w3);
endmodule

module Full_Adder_4 (sum, c_out, a, b, c_in);
  output [3:0]sum;
  output c_out;
  input [3:0] a, b;
  input c_in;
  wire c_in2, c_in3, c_in4;
  Full_adder M1 (sum[0], c_in2, a[0], b[0], c_in);
  Full_adder M2 (sum[1], c_in3, a[1], b[1], c_in2);
  Full_adder M3 (sum[2], c_in4, a[2], b[2], c_in3);
  Full_adder M4 (sum[3], c_out, a[3], b[3], c_in4);
endmodule
What’s after RTL synthesis?

Results
(Design Productivity)

Effort
(EDA tools effort)

1978
1985
1992
1999

1999 1999 1999 1999

McKinsey S-Curve

Transistor entry

Schematic Entry

RTL Synthesis

What’s next?
Current Practice: HDL at RTL Level

module foobar (q,clk,s,a,b);
    input clk, s, a, b;
    output q; reg q; reg d;
always @(a or b or s) // mux
begin
    if( !s )
        d = a;
    else if( s )
        d = b;
    else
        d = 'bx;
end // always @(a or b or s)
always @(clk) // latch
begin
    if( clk == 1 )
        q = d;
    else if( clk !== 0 )
        q = 'bx;
end // always @(clk)
endmodule
RTL Synthesis Flow

module Full_Adder_4 (sum, c_out, a, b, c_in);
output [3:0] sum;
output c_out;
input [3:0] a, b;
input c_in;
wire c_in2, c_in3, c_in4;
Full_adder M1 (sum[0], c_in2, a[0], b[0], c_in);
Full_adder M2 (sum[1], c_in3, a[1], b[1], c_in2);
Full_adder M3 (sum[2], c_in4, a[2], b[2], c_in3);
Full_adder M4 (sum[3], c_out, a[3], b[3], c_in4);
endmodule
Cover All Aspects of the Design Process

- **Design**: specify and enter the design intent

**Verify**: verify the correctness of design and implementation

**Implement**: refine the design through all phases
Lecture Overview

- Introduction to Kurt, Sanjit, .... and others
- Education and your future career
- CAD, Semiconductors and the broader economy
- Brief overview of CAD
- Goals of course
Goals of Course

- Help to develop the core competences of a CAD engineer
  - Software expertise
  - Algorithmic facility
  - Domain expertise in ic design
- Communicate the essence of the current IC design flow in a semester
  - Goal: “If Avanti, Cadence, and Synopsys employees were all abducted by aliens, their software could be recreated by this class.”
- Prepare you for performing publishable research – aim high, a real publication!
Something for Everyone

- Processing, Devices students – understand the tool flow, examine ways of bridging the gap between processing, design, and CAD
- Circuits students – understand how the tools that you will be using for the rest of your life work
- CAD students – give you foundation material for the field, prepare you for preliminary examinations
- Theory types – understand how algorithms are applied in this algorithm-rich area
Approach of the Course

- Each week
  - Examine a portion of the IC design flow
  - Identify one or more key problems
  - Formulate the problem mathematically
  - Solve the problem, examining trade-offs between
    - The computational efficiency of the algorithms
    - The quality/optimality of the result
  - Look at contemporary practice
  - See how close the classroom work approaches industrial practice
Course logistics

- EECS 244
- Cory 540A/B, Monday, Wednesday 2:30 – 4:00 PM
- Prof. Kurt Keutzer, Cory 566, Office hour: Monday 4:00–5:00PM, or by appointment
  - Keutzer at eecs.berkeley.edu
- Prof. Sanjit Seshia, Cory 568 sseshia at eecs.berkeley.edu
- Course reader at Copy Central, 2483 Hearst Avenue, near Euclid
- Recommended book: Logic Synthesis, Devadas, Ghosh, Keutzer – buy from Amazon.com
- Exam 1: 30%
- Exam 2: 30%
- Final project: 40% (20% general content, 10% content in presentation, 10% content in written report)
- No TA for course

- Syllabus, Web page up now
  http://www-cad.eecs.berkeley.edu/~keutzer/classes/244fa2005/244fa2005-h6.htm
- The course material will not be hard for you – but the project may be …