Linearly graded doping drift region: a novel lateral voltage-sustaining layer used for improvement of RESURF LDMOS transistor performances

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Received 5 February 2002, in final form 17 May 2002
Published 18 June 2002
Online at stacks.iop.org/SST/17/721

Abstract
A linearly graded doping drift region structure, a novel lateral voltage-sustained layer used for improvement of reduced surface field (RESURF) LDMOS transistor performance has been evaluated theoretically, numerically and experimentally in this paper for the first time. Due to the coupling effect of the two-dimensional (2D) electrical field, it is found from the theory developed here that the linearly graded drift region-doped profile can provide a high breakdown voltage while maintaining a high doping dose in the total drift region for minimizing the on-resistance $R_{on}$. The characteristics of such an LDMOS have been demonstrated by the 2D semiconductor device simulator MEDICI and further verified by our experimental results. We have obtained a reduction of the on-resistance of 50\% from 10.3 m\Omega cm$^2$ to 5 m\Omega cm$^2$ in the on-state, and an increase of the breakdown voltage by a factor of 2.5 from 90 V to 234 V in the off-state, compared to the values for conventional RESURF devices. The experimental results verify the performance improvement predicted by the simulation and theory.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

High-voltage integrated circuits which typically combine one or more high-voltage transistors on the same chip with low-voltage circuits are widely used in various electric applications, such as telecommunication, electronic luminescent displays and lamp ballasts, etc. In these circuits, a so-called lateral double-diffused MOS transistor (LDMOS) is the most important conventionally used high-voltage device. In the practical design of the LDMOS transistor, it is a fundamental requirement to minimize the on-resistance while still maintaining a high breakdown voltage. However, these two electrical parameters often conflict with each other in the present day processing technology. For instance, the conventional reduced surface field (RESURF) technique can not only produce a high breakdown voltage but also a high on-resistance [1, 2]. Although many methods, such as the multiple-resistivity drift region technique [3], surface ion implantation in the drift region and use of an SIPOS resistance layer on the oxide layer have been proposed to reduce the on-resistance [4, 5], no considerable improvement has been obtained. In this case, optimization of the device parameters is very important to obtain an acceptable trade-off between the voltage blocking capability and the on-resistance [6–8].
In the early bulk silicon technology, a lateral non-uniform doping profile was used to avoid low breakdown voltage caused by the radius of curvature of the metallurgical junction [9]. Continuous graded junction terminations [10, 11] were also used for the same purpose. Extending the reduced surface field (RESURF) principle to silicon-on-insulator (SOI) technology, Merchant et al. developed a theoretical model for optimizing the breakdown voltage of thin film SOI RESURF LDMOS transistors [12], which predicted that the linear lateral doping profile in the drift region on SOI could be designed to attain maximum breakdown voltage [13, 14]. A computer program was developed to realize this profile and experimental verifications were also performed [15, 16]. However, these results were only available for thin film SOI RESURF LDMOS devices. As is well known, the advantages and applications of thin film SOI technology using the RESURF principle are countered somewhat by high cost of the SOI substrate materials and self-heating of the high-voltage power devices.

In this paper, the non-uniform lateral doping profile is employed once again with bulk silicon technology to produce junction isolation RESURF LDMOS devices. Based on modulation of the lateral electric field distribution in the drift region rather than the traditional junction termination shaping, a novel lateral voltage-sustained layer with a linearly graded doping region is proposed for the junction isolation RESURF LDMOS transistor, and an analytical theory is developed based on the two-dimensional Poisson equation. Following this, a RESURF LDMOS transistor with such a linearly graded drift region-doped profile has been simulated by the 2D semiconductor device simulator MEDICI and implemented practically. The numerical analysis and experimental results illustrate that this novel device has an improved trade-off between the breakdown voltage and on-resistance compared to conventional constant drift region doping structures, verifying our theoretical predictions. We believe that use of this novel structure in high voltage and SPIC circuits can significantly improve system performance.

2. Theory

A simplified schematic cross section of the RESURF LDMOS transistor is shown in figure 1. In the present analysis, the epilayer length of the drift region is defined as the n-type region length \( L \) between the n+ drain and p+ well. The epilayer thickness is \( t_1 \) with a doping concentration profile of \( N_d(x) \). We assume that the substrate is thick enough to deplete the substrate charge. The substrate doping concentration is \( N_{sub} \) as the depletion layer thickness \( t_2 \), the thickness of the field oxide layer \( t_o \), the dielectric constant \( \varepsilon_{ox} \), and the horizontal and vertical positions relative to the silicon surface are \( x \) and \( y \), respectively. The device is biased in the off-state configuration; substrate, source and gate are grounded while the drain is biased to a positive voltage \( V_d \).

As shown in [14], the ionization path may be taken as the horizontal path, assuming that the depletion region reaches the drain diffusion. The ionization integral may be written as

\[
I[\phi_l(x)] = \int_0^L (\phi_l(x)) \, dx
\]  

where \( \phi_l(x) \) is the electrostatic potential along the top surface of the drift region, \( \alpha[\phi_l(x)] \) is the ionization rate and \( E(x) = \phi_l(x) - \phi_h(x) \) is the magnitude of the lateral electric field in \( V/cm \).

An optimum RESURF structure would have the least ionization for a given drift length and drain voltage. The \( \alpha[\phi_l(x)] \) that minimizes \( I \) for a given \( V_d \) and \( L \) is the solution of Euler’s equation

\[
\frac{d}{dx} \left( \frac{d\phi_l(x)}{dx} \right) = 0.
\]  

In the case of a power law for the effective ionization rate, we have

\[
\alpha[\phi_l(x)] = A \cdot e^{-B/\phi_l(x)}.
\]  

As shown in [14], equations (2) and (3) imply that

\[
\phi_l(x) = kx.
\]  

Thus, the optimum RESURF device would have a uniform lateral electric field profile \( E = \frac{V_d}{L} = k \). As a result, we obtain

\[
\phi_l(x) = \frac{V_d}{L} x.
\]  

It is well known that an avalanche breakdown occurs when the ionization integral equals 1. Our treatment is not the same as that in [14], and the well-known Fulop’s formula [17] for silicon materials is adopted here

\[
\alpha_{eff} = AE^2\]

with \( A = 1.8 \times 10^{-35} \, cm^{-1} \). The ideal breakdown voltage and the critical field are found to be

\[
V_b = \left( \frac{L^5}{A} \right)^{1/7} \]  

\[
E_C = \left[ \frac{L^{-1}}{A} \right]^{1/7}.
\]

The ideal breakdown voltage and critical peak field for the ideal doping profile and the uniform doping profile are plotted in figure 2. For the sake of comparison, the results of the
equation a 1D equation describing the surface potential in the box drift region. It is possible to derive from the 2D Poisson profiles, respectively. (with good agreement between different treatments. The potential function \( \phi(x, y) \) in the drift region of the silicon film must be satisfied by the Poisson equation, yielding

\[
\frac{\partial^2 \phi(x, y)}{\partial x^2} + \frac{\partial^2 \phi(x, y)}{\partial y^2} = -\frac{qN_d(x)}{\varepsilon_{Si}}. \tag{9}
\]

As shown in figure 1, the region under investigation is a box drift region. It is possible to derive from the 2D Poisson equation a 1D equation describing the surface potential in the lateral coordinate \( z \). In this work, a more general analysis integrates the Poisson equation over the \( y \)-direction in the drift region

\[
\int_0^{t_1} \frac{\partial^2 \phi(x, y)}{\partial x^2} \, dy + E_y(x, 0) - E_y(x, t_1) = -\frac{qN_d(x)}{\varepsilon_{Si}}. \tag{10}
\]

Under the assumption of a 1D electrical field in the SiO\(_2\) material, the continuity of electrical flux along the Si/SiO\(_2\) interface makes the boundary conditions for (9) satisfy

\[
E_y(x, 0) - E_y(x, t_1) = -\frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\phi(x, t_1)}{t_1} \tag{11}
\]

where \( \phi(x, t_1) = \phi(x, 0) \) is the potential function along the Si/SiO\(_2\) interface, \( V'_{gs} = V_{gs} - V_{FB} \) is the effective gate-to-source bias voltage, and \( V_{FB} \) is the channel flat-band voltage.

Because the gate oxide layer and substrate bias equal zero, neglecting the influence of the work function difference between the metal and semiconductor on the electric field, the electric field at the interface can be approximated by

\[
E_y(x, 0) \approx -\frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\phi(x, t_1)}{t_1}. \tag{12}
\]

Combining (10) with (12), we obtain

\[
\int_0^{t_1} \frac{\partial^2 \phi(x, y)}{\partial x^2} \, dy - \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\phi(x, t_1)}{t_1} = -\frac{qN_d(x)}{\varepsilon_{Si}}. \tag{13}
\]

According to the RESURF principle, the epilayer should be completely depleted and the depletion approximation suitable for the drift region. To a first-order approximation, the integral term of (13) can be reduced to a function of the front surface potential by assuming \( \frac{\partial^2 \phi(x, y)}{\partial x^2} \approx \frac{\partial^2 \phi(x, t_1)}{\partial x^2} \). This approximation generally exists for the depleted structure, as shown in [18, 19].

The relationship between \( \phi_1(x) \) and \( \phi_0(x) \) derived by solving the Poisson’s equation (9) in the vertical direction through the above approximation is thus

\[
\phi_1(x) = \phi_0(x) + E_y(x, t_1)t_1 - \frac{qN_d(x)}{2\varepsilon_{Si}} \frac{\partial^2 \phi_0(x)}{\partial x^2} \tag{14}
\]

where \( \phi_0(x) \equiv \phi(x, t_1) \) is defined as the electrostatic potential at the metallurgical junction of the vertical n\( ^-\)/p\( ^+\) junction.

From basic p–n junction theory, \( \phi_0(x) \) can be simplified to

\[
\phi_0(x) = -\frac{qN_{sub}}{2\varepsilon_{Si}} f_2. \tag{15}
\]

Putting (14) and (15) into (13) and after further mathematical simplification, (13) is transformed into the 1D differential equation

\[
\frac{\partial^2 \phi_1(x)}{\partial x^2} - \alpha_l \phi_1(x) = \beta_l \tag{16}
\]

where

\[
\alpha_l = \frac{2\varepsilon_{ox}}{t_1 t_1 t_1} + \frac{q}{2\varepsilon_{Si}} N_d(x) + N_{sub} \left( \frac{t_1}{t_1} \right)^2 \]

\[
\beta_l = \frac{q}{2\varepsilon_{Si}} N_d(x) + N_{sub} \left( \frac{t_1}{t_1} \right)^2. \tag{17}
\]

In order to determine the depletion layer thickness on the substrate side, we must solve for the potential distribution of the double-sided p–n junction in the vertical direction. Assuming the depletion width along the drift region length direction to be uniform, the general formula of the double-sided junction for the applied drain voltage \( V_d \) can be given by

\[
V_d = \phi_d + qN_{sub}t_2 \frac{t_1}{2\varepsilon_{Si}} = \frac{qN_{sub}t_2}{\varepsilon_{Si}}. \tag{17}
\]

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Combining (15) with (17), we obtain the quadric equation

$$\frac{t_2}{t_1} = \sqrt{1 + \frac{N_{d}(x)}{N_{sub}} + \frac{2e_{ox}V_d}{qN_{sub}t_1^2t_2} - 1}. \quad (18)$$

It is evident that $t_2$ tends to zero when the substrate doping concentration $N_{sub}$ tends to a very high value, such as infinity. The above form is only applicable for the condition when the drain voltage makes the depletion width larger than $t_1$. For RESURF LDMOS devices, this condition is always valid. As a result equation (16) becomes

$$\frac{d^2\phi(x)}{dx^2} = -\frac{2}{t_1^2} + \frac{2e_{ox}}{t_1qN_{sub}}\phi(x)$$

$$= \frac{q}{\varepsilon_{Si}}N_{d}(x) + N_{sub}\left[1 + \frac{N_{d}(x)}{N_{sub}} + \frac{2e_{ox}V_d}{qN_{sub}t_1^2} - 1\right]^2. \quad (19)$$

Assuming that the RESURF LDMOS structure has an optimum doping profile, from equation (4) and the uniformity of the electric field we obtain

$$\frac{d^2\phi(x)}{dx^2} = -\frac{dE(x)}{dx} = 0. \quad (20)$$

Inserting (20) into (16) gives

$$\phi(x) = \frac{q}{2\varepsilon_{Si}} \left[N_{d}(x) + N_{sub}\left(\frac{t_2}{t_1}\right)^2\right]^{\frac{1}{2}}t_1^2t_2\frac{t_2}{t_1q}\varepsilon_{ox}/\varepsilon_{Si} + t_1. \quad (21)$$

Finally, combining (5) and (21), we obtain

$$N_{d}(x) = \frac{2e_{ox}(t_1q\varepsilon_{ox}/\varepsilon_{Si} + t_1)V_d}{q^2t_1^2L} - N_{sub}\left(\frac{t_2}{t_1}\right)^2. \quad (22)$$

As shown in (22), the ideal drift region doping profile for maximum breakdown voltage is a linearly graded function, with an amplitude related to the drift region length, epilayer thickness, field oxide thickness and substrate doping concentration. Moreover, the optimum doping gradient can be obtained by differentiating (22) with respect to $x$:

$$G = \frac{2e_{ox}(t_1q\varepsilon_{ox}/\varepsilon_{Si} + t_1)V_d}{q^2t_1^2L}. \quad (23)$$

Based on the above theoretical analysis, we can draw a very useful conclusion: to obtain the maximum breakdown voltage and thus an improved trade-off, the linearly graded drift region-doping profile is the ideal choice. For such LDMOS transistor structures, the procedure for obtaining the optimum design parameters is as follows. For a given breakdown voltage $V_d$ the required drift region length $L$ is calculated by using (7); following the determination of the field oxide thickness $t_1$ and the epitaxial thickness $t_2$, the slope of the linear doping profile $G$ is obtained from (23), thus the maximum doping concentration $N_{d}(L)$ in the drift region can be obtained. Solving the equations (18) and (22) then gives the substrate doping concentration $N_{sub}$ and the required smallest depletion layer thickness $t_2$ in the substrate. For instance, the drain region length for BV = 250 V is 12 µm; the slope of the linear doping profile is $1.72 \times 10^{10} \text{cm}^{-2}$ from (23) for a field oxide thickness of 4500 Å and an epitaxy thickness of 4 µm. The remaining parameters can also be determined following the above procedure, e.g., the maximum doping concentration in the drift region is found to be $2.1 \times 10^{16} \text{cm}^{-3}$ and the implantation dose about $1.2 \times 10^{12} \text{cm}^{-2}$. The substrate doping concentration is determined to be $1.8 \times 10^{15} \text{cm}^{-3}$ for the substrate.

The following sections describe the numerical analysis and experimental verification obtained by the TMA MEDICI simulations and the implementation of such a RESURF LDMOS transistor.

### 3. Simulation

The cross-sectional view of the proposed RESURF LDMOS is already shown in figure 1. The device parameters are listed in table 1 based on the calculation in the above section for a breakdown voltage of 250 V. The linearly graded drift region-doping profile of $N_{d}(x)$ in the proposed LDMOS is matched by multiple stepwise variation of the uniform doping concentration with different lengths. In practical devices, the linearly graded drift region-doping profile can be created using a single phosphorus implant through a mask with a series of openings that are smaller near the source and larger near the drain [11]. For the sake of comparison, a conventional RESURF LDMOS structure with a constant drift region doping concentration $1 \times 10^{15} \text{cm}^{-3}$ and epilayer thickness of 4 µm is simultaneously considered, with a drift region length of 12 µm and substrate doping concentration of $2 \times 10^{15} \text{cm}^{-3}$. The structure parameters used in the simulation are also shown in table 1. The source and drain doping concentrations are $1 \times 10^{20} \text{cm}^{-3}$, while the doping profile of the p-base region is a Gaussian function with a surface doping concentration of $1 \times 10^{18} \text{cm}^{-3}$ and junction depth of 3.2 µm. The ratio of lateral/vertical diffusion is assumed to be 0.8. The other parameters in both structures are the same unless a special note is given.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Conventional LDMOS</th>
<th>Proposed LDMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate doping concentration $N_{sub}$ (cm$^{-3}$)</td>
<td>$2 \times 10^{15}$</td>
<td>$2 \times 10^{15}$</td>
</tr>
<tr>
<td>Drift region-doped concentration $N_{d}$ (cm$^{-3}$)</td>
<td>$1 \times 10^{15}$</td>
<td>$1 \times 10^{15}(1 + 10^4x/L)$</td>
</tr>
<tr>
<td>Epitaxial layer thickness (µm)</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Drift region length (µm)</td>
<td>12</td>
<td>12</td>
</tr>
</tbody>
</table>

Table 1. Device structure parameters used in the numerical simulation.
Linearly graded doping drift region

Figure 3. Simulated blocking capability of (a) conventional RESURF LDMOS with a constant drift region doping of $1 \times 10^{15}$ cm$^{-3}$ and contours = 10 V/step, and (b) proposed RESURF LDMOS with a drift region doping of $1 \times 10^{15} (1 + 10^4 x/L)$ cm$^{-3}$ and contours = 24 V/step.

the extracted ionization integral equal to 1, the avalanche breakdown voltages can be readily obtained. As observed in this figure, the breakdown voltage of the conventional RESURF LDMOS is limited to 90 V, which is due to the enhanced surface peak field near the drain edge. When the breakdown voltage for the linearly graded doping-drift region RESURF LDMOS is 234 V, an enhancement factor of 2.5 is obtained because the smooth profile of the surface electrical field significantly decreases the surface peak field near the source and drain edges. It should be noted that the potential contour lines near the drain in the new structure are smoothed away in figure 3(b), while they are crowded at the edge of the drain in figure 3(a) for conventional LDMOS structures.

The simulated one-dimensional field distributions in top silicon–field oxide interfaces are illustrated in figure 4, where the surface electrical field distribution of the linearly graded drift region-doped LDMOS is more or less uniform in the entire drift region, leading to an enhanced breakdown voltage of 240 V. In contrast, the electrical field appears to be non-uniform in the conventional RESURF LDMOS, as shown in figure 4(b). The peak field reaches a critical electrical field magnitude of $2.3 \times 10^5$ V cm$^{-1}$ at the drain edge, giving rise to a breakdown voltage of 90 V.

Figure 5 demonstrates the results of the simulated potential distributions at breakdown. We can see from figure 5(a) that it is just the linearly graded distribution of the surface potential that leads to the uniform field profile in most of the drift region of the linearly graded drift region-doped LDMOS, as shown by our theory. The two peak fields at the edges of the source and drain are strongly related to the effect of the diffusion radius of curvature of the metallurgical junction, as shown in [20]. In contrast, the potential distribution of the conventional RESURF LDMOS shows a large curvature in the whole drift region, as shown in figure 5(b), which leads to a non-uniform electrical field profile Consequently, the breakdown voltage suffers a considerable degradation.

The specific on-resistance $R_{on}$ can be extracted from the simulated forward characteristics in the linear region of the $I$–$V$ curves of the LDMOS. We find that the linearly graded
Figure 4. Electrical field distribution near the silicon film/field oxide layer interface of (a) linearly graded doping drift region RESURF LDMOS and (b) conventional RESURF LDMOS.

Figure 5. Potential distribution at the silicon film/field oxide layer interface of (a) linearly graded doping drift region RESURF LDMOS and (b) conventional RESURF LDMOS.

Figure 6. Trade-off between the breakdown voltage and on-resistance $R_{on}$ as a function of the drift region length for linearly graded doping drift region and conventional RESURF LDMOS transistors.

4. Experimental results

The simulation results were verified by experimental realization of the optimal linearly graded drift region-doped RESURF LDMOS. It was found that a continuous lateral linearly graded doping profile can be achieved by using a layer of oxide or photoresist with a sequence of slit openings for masking of the impurity implantation [11]. These slits are continuously smaller toward the p$^+$/n$^-$ junction from the n$^-$ side. All design details for implementing the linear doping profile in the device drift region may be found in [15].

A 200 V CMOS compatible LDMOS process was designed using the T-SUPERM-IV and implemented. The silicon material used was (100)-oriented with a substrate doping concentration of $2 \times 10^{15}$ cm$^{-3}$. After epitaxial growth of the drift region of 4 $\mu$m thickness with a doping concentration of $1 \times 10^{15}$ cm$^{-3}$, the process began by silicon mesa formation using reactive ion etching. Then, a 0.1 $\mu$m thick LTO was deposited, followed by photo-resist deposition on the drift region mask to define the silicon width and slit spacing. Phosphorus was then implanted into the silicon layer to form the drift region, with an implantation energy of 100 keV and a dose of $6.1 \times 10^{12}$ cm$^{-2}$ for the drain region. After photo-resist stripping, a 400 nm thick LTO was deposited to prevent impurity out-diffusion into the ambient during the
Linearly graded doping drift region

A novel lateral voltage-sustained layer with linearly graded doping drift region has been evaluated and an analytical model developed. It has been shown that an optimal linearly graded drift region-doping profile for the RESURF LDMOS transistor can lead to a uniform distribution of the surface electric field as well as a linearly graded electrostatic potential, resulting in low on-resistance and high breakdown voltage. The significant characteristics of the RESURF LDMOS proposed here have been well demonstrated by the semiconductor device simulator MEDICI and verified by experimental results.

5. Conclusion

The authors would like to thank all referees for their helpful comments and good suggestions.

Acknowledgments

References

[10] Steng R and Gosele U 1985 Variation of lateral doping—a novel concept to avoid high voltage breakdown of planar junctions IEDM ’85 Tech. Dig. 154–7


