Accurate In Situ Measurement of Peak Noise and Delay Change Induced by Interconnect Coupling

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Abstract—An accurate in situ noise and delay measurement technique that considers interconnect coupling effects is presented. This paper improves upon previous work by proposing 1) a novel accurate peak detector to measure on-chip crosstalk noise, and 2) in situ measurement structure to characterize the dynamic delay effect. A test chip was fabricated using 0.35-μm process and measured results demonstrate the effectiveness of the proposed technique. Noise peak measurements show 40–60 mV (1.8% average) accuracy to simulation results and dynamic delay change curve match well with SPICE. The proposed measurement technique can be used for interconnect model verification and calibration, and has applications to various design automation tools such as noise-aware static timing analysis.

Index Terms—Crosstalk, delay effects, integrated circuit interconnections, noise measurement, peak detectors.

I. INTRODUCTION

In the deep-submicron regime, interconnect coupling noise is one of the greatest concerns for circuit designers due to high clock frequencies and accelerated interconnect scaling. The accuracy of the interconnect models, tools, and design guidelines are critical to meeting the strict specifications and tight design schedule of high-performance chips. Therefore, interconnect model error should be carefully controlled. To verify and calibrate existing interconnect models, an accurate noise measurement scheme is lacking.

Coupling noise has two distinct impacts on the circuit function: false switching and dynamic delay. To cope with the false switching problem, analytical models to predict peak coupling noise height have been proposed [1], [2]. To handle dynamic delay problems in timing simulation, methodologies for noise-aware static timing analysis (STA) are beginning to be presented [3], [4]. The above models must continuously be enhanced and calibrated to measurement results from fabrication lines.

However, coupling noise effects of on-chip interconnect are difficult to measure since they are highly sensitive to external probing. For the accurate measurement of these phenomena, in situ time-domain techniques [5] can recreate on-chip waveforms without uncertainties arising from the parasitics of a direct probing. A wide-range comparator (WRC), with near-rail-to-rail operation range [6], translates signal delay into a simple transition at the output pads.

In this paper, we improve upon an in situ measurement technique to accurately evaluate subnanosecond on-chip coupling effects. Specifically, we aim to characterize the peak noise height and coupling induced delay variation for varying metal levels, pitches, and driver characteristics. We improve upon [5] in the following ways.

• We propose a novel and more accurate method of measuring peak noise.
• We draw comparisons between measurement results, SPICE, and analytical models of peak noise.
• We investigate the impact of noise on delay.
• We vary aggressor and victim signal arrival times as well as drive strengths independently.

II. IN-SITU MEASUREMENTS OF INTERCONNECT COUPLING EFFECTS

A. Overall Measurement Structure

Fig. 1 illustrates the simplified block diagram of an in situ measurement site in this work. In the test structure, coupling noise is caused by two aggressor lines located on each side of the victim line. Nodes $A_{in}$ and $V_{in}$ are the aggressor and victim signal inputs, respectively. After each signal is sufficiently buffered, variable impedance drivers [7] are used to drive the lines. The waveforms on the victim path are sampled by one of two types of comparators and propagated to the pads. The mode signal selects the comparator to be used depending on the type of measurement being performed: signal delay measurement or noise peak height measurement.

Both dummy gates and comparators act as normal output loads which a gate would see in an actual design. The dummy gates are placed wherever necessary to maintain identical buffer
B. Peak Noise Height Measurement Circuits

A primary goal of our work is to capture the crosstalk noise peak height accurately. A WRC has insufficient bandwidth to capture peak noise height in subnanosecond pulses. Even mildly sharp noise waveforms will be distorted, resulting in 20%–30% error in the noise peak value. Therefore, in [5], the authors were forced to limit their noise peak analysis to very long, resistive interconnects with wide pulsewidths (1–3 ns at half-maximum or 2–8 ns at the base) and large noise peaks. In this paper, we focus on realistic global and semiglobal interconnections that can be found in actual high-performance designs.

As more advanced processes yield sharper noise pulses, an improved noise detection circuit is necessary. An accurate peak detector (APD) circuit, composed of a cascaded low-gain high-speed differential amplifier as a comparator and a pseudo-dynamic latch circuit, is developed in this work. A schematic diagram of the APD is shown in Fig. 2(a). We use a five-stage cascade of low-gain differential amplifiers as a comparator. The triangles represent source-coupled nMOS differential amplifiers. Stage gain was designed to be around 2 to 3 to achieve the high bandwidth necessary to capture sharp noise peaks. After an appropriate level shift to restore full swing at the amplifier outputs, both φ and θ are used as clock signals for the latch to hold the value at the output pads. This is required since the output pulsewidth can be as narrow as 100 ps when the reference voltage is near the peak value.

In this measurement, the aggressors are switched while the victim input is held at Vref. We use the APD to compare a reference voltage Vref to the far-end noise at node vf. When the noise waveform crosses the reference voltage, out2 switches as shown by the solid line in Fig. 2(b). The peak height of the noise waveform is measured by sweeping the reference voltage and applying the reset signal for the latch circuit between measurements. Switching stops when the waveform does not cross the reference, as shown by the dashed line. The noise peak is thus found to be the lowest reference voltage that switches the latch. Using this structure, the noise peak is easily translated into a relatively slow signal transition at the output pads that is easy to measure.

Fig. 3 shows results from SPICE simulations of the sensitivity of the APD. The detection error is defined as the difference between the measured peak voltage and actual peak voltage. The dotted lines show Tc, the duration of the time that the noise waveform is smaller than the reference voltage (i.e., the noise magnitude exceeds the user-defined threshold). The APD circuit in our 0.35-μm process captures a noise pulse when the Vref crossing time Tc is 130 ps or more. For a nominal coupling noise of 0.4-V height and 1-ns base width (based on recent technologies), the APD requires approximately 100-ps crossing time, yielding a 40-mV detection error (10% error, in this case). This analysis is pessimistic since actual noise waveforms are flatter at the peak than the triangular pulse used.

In summary, the dedicated comparator achieves significant performance improvements over a wide-range comparator in simulation results. For noise pulses with less than 2–2.5-ns base width, the APD is necessary to limit measurement error.

1This translates roughly to sub-1-ns half-maximum noise pulsewidths.
TABLE I
TECHNOLOGY SUMMARY

<table>
<thead>
<tr>
<th>Process</th>
<th>0.35 μm, 4-metal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal 1–3 minimum pitch</td>
<td>1.2 μm</td>
</tr>
<tr>
<td>Metal 4 minimum pitch</td>
<td>2.4 μm</td>
</tr>
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<td>Driver impedance</td>
<td>96 – 703 Ω (7 steps)</td>
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<tr>
<td>Chip area</td>
<td>7.1 x 2.2 mm²</td>
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<tr>
<td>No. of test sites</td>
<td>14</td>
</tr>
</tbody>
</table>

C. Delay Change Measurement Circuits

The time-domain technique of [5] is used as the basis for measuring the impact of coupled noise on victim line delay. The objective of this measurement is to characterize the delay change as a function of the relative arrival times of the aggressor and victim inputs. The mode signal in Fig. 1 selects the WRC circuit. Setting the reference voltage to VRef, the internal delay of the victim line including the driver can be calculated by comparing the delay at the output pads out0 and out2. Alternatively, pure wire delay can be found by examining out1 and out2.

To investigate the victim delay change, switching input pulses are supplied to both the aggressor and victim drivers. Independent control of the aggressor and victim signal inputs allows us to measure the impact of the relative arrival timing difference between the two. Also, our setup uses independently controllable variable impedance drivers for victim and aggressors, enabling us to experimentally characterize this effect on timing and noise for the first time.

III. TEST CHIP IMPLEMENTATION

To evaluate the effectiveness of the proposed structures and circuits, a test chip was fabricated using a 0.35-μm four-metal process. The features of the test chip are summarized in Table I and a die photograph is shown in Fig. 4.

Line length, metal levels, and pitches are varied over the 14 measurement structures. To investigate and evaluate closed-form noise models, both the aggressor and victim driver sizes, as well as their signal-edge alignment, were controlled to reflect the wide range of neighboring wire possibilities found in actual chips. On-chip calibration structures are implemented for the WRC and APD circuits to eliminate process-dependent offsets and extract delay characteristics of the WRC at different reference voltages. No special instruments are required in the measurements, since the sensitive signals are converted inside the chip to robust digital signals and propagated to the pad.

IV. EXPERIMENTAL RESULTS

A. Noise Peak Measurement

Fig. 5 illustrates the dependency of peak noise height on victim driver on-resistance for a metal-4 6-mm global interconnect. Aggressor driver on-resistance is fixed at a relative strength of 7 (Ron = 96 Ω), while the victim driver on-resistance varies over the relative strength range 1–7. The peak noise voltage is normalized to Vdd (3.3 V).

In Fig. 5, the simulation results match measurement data well. The maximum discrepancy is less than 3% of Vdd, with the average difference less than 60 mV. Average relative error between measurement and SPICE is 7.5%. The error can be further calibrated using noise width information from delay variation measurements, which will be detailed in the Section IV-B. Note that the narrower linewidth in Fig. 5 experiences a higher noise peak due to its larger resistance and ratio of coupling capacitance to total capacitance (despite identical line spacings). Smaller victim driver sizes also contribute significantly to a larger noise peak. This result suggests the on-resistance of the driver as well as the interconnect resistance should be optimized when a long coupling length cannot be avoided.

Table II compares peak noise data from the proposed technique, SPICE simulation, and the analytical crosstalk model in [2]. In this case, the interconnect configuration is a minimum pitch metal-4 6-mm line. Results are presented for seven possible victim strengths using a fixed aggressor strength of 7. The numbers in parentheses show the differences compared to measurement results. Good agreement is found for all data within a few percent. Even in the case of a strong victim when the noise peak will be sharpest, the data matches well. The estimated half-maximum noise pulsewidths in our measurements are in the range of 0.25–0.85 ns, compared with 1–3 ns in [5].

Fig. 5 and Table II suggest that the proposed measurement technique may consistently clip the noise peak. However, the voltage clipped remains less than 2.5% of the supply voltage (<80 mV for 3.3 V) for noise pulses wider than 0.25 ns. In Fig. 6, we plot the relative error between measurement and SPICE against the simulated noise pulse half-maximum width. Appreciable error (10%–16%) occurs only for noise...
pulses narrow than 0.35 ns and even then our results compare favorably to previously published reports of 20%–30% error at 1-ns noise widths [5].

Our technique can be extended to measure inductive coupling effects in bus structures by activating dummy lines in Fig. 1. A significant inductive impact was not observed for the process and driver sizes used in these designs according to simulation. General cases with multiple aggressors can also be measured with independent control of each aggressor, partial coupling lengths, etc. Furthermore, the APD approach to noise peak measurement should scale well since comparator bandwidth increases directly with device speed improvements, yet noise peak bandwidth does not always. Based on simulations, noise pulse bandwidth (inversely proportional to noise pulsewidth) scales along with gate speed for buffered global wires, since buffer insertion balances gate and wire delays. However, scaling unbuffered semiglobal wiring yields a linear increase in wire RC delay despite shrinking wirelengths. The result is a sublinear increase (with respect to gate speed) in noise bandwidth for semiglobal wiring. The scalability of our measurement technique is particularly good in these instances, while accuracy remains relatively unchanged in buffered global wiring due to its similar scaling properties with the APD.

### B. Dynamic Delay Change Measurement

The measured impact of coupling noise on delay for 3-mm metal-3 lines is shown in Fig. 7. The delay change is plotted as a function of relative signal arrival times of the aggressor and victim \((T_a - T_v)\). Changing relative signal arrival times alters the victim line delay due to the varying coupling capacitance between parallel lines. We refer to this depiction of dynamic delay as a delay change curve (DCC). DCCs tell designers and routing tools how much extra setup and hold margin is required for receiver latches. A description of the fundamental relationship between DCCs and coupled noise waveforms as discussed in Section III can be found in [8].
Fig. 7(b) includes two victim driver cases of strength 1 and 2, with a fixed aggressor strength of 7. For each case, two possible combinations of aggressor and victim signal input directions, as shown in Fig. 7(a), are supplied. The peak-to-peak delay change exceeds 400 ps for a victim relative strength of 1, and 200 ps for a strength of 2, which is ±30% and ±20% variation around the nominal delay, respectively.

Increasing the victim driver size is one way of minimizing dynamic delay. The measured peak-to-peak delay change and base width of the coupling noise as functions of the driver size are shown in Fig. 8. In the figure, both the peak-to-peak delay change and base width decrease rapidly when a larger driver is used. Charge injected onto the victim net must be removed through the interconnect and driver resistances. The large slope of the curves where the driver is small implies that the on-resistance of the driver dominates. The curve saturates when the driver strength is 4 or above. At this point, the interconnect resistance is 62% of the total victim resistance and limits the speed at which the victim driver can remove injected charge.

V. Conclusion

An accurate in situ measurement technique for noise peak height and delay change due to interconnect coupling is proposed. Using this new characterization method, noise height is measured with 40–60-mV accuracy. We also clarify the impact of the relative input timing of the aggressor and victim on the victim delay margin. The experimental results measured using a 0.35-μm process demonstrate the effectiveness of the proposed technique.

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REFERENCES