Hot-Carrier Reliability Comparison for pMOSFETs With Ultrathin Silicon-Nitride and Silicon-Oxide Gate Dielectrics

Igor Polishchuk, Student Member, IEEE, Yee-Chia Yeo, Student Member, IEEE, Qiang Lu, Student Member, IEEE, Tsu-Jae King, Member, IEEE, and Chenming Hu, Fellow, IEEE

Abstract—The degradation of 100-nm effective channel length pMOS transistors with 14 Å equivalent oxide thickness Jet Vapor Deposition (JVD) Si$_3$N$_4$ gate dielectric under hot-carrier stress is studied. Interface-state generation is identified as the dominant degradation mechanism. Hot-carrier-induced gate leakage may become a new reliability concern. Hot-carrier reliability of 14 Å Si$_3$N$_4$ transistors is compared to reliability of 16 Å SiO$_2$ transistors.

Index Terms—Degradation mechanism, interface states, stress-induced leakage current, substrate current.

I. INTRODUCTION

As GATE-OXIDE thickness in MOS devices is reduced, the increasing gate leakage current poses a major challenge to continued transistor scaling. Reliability of the ultrathin SiO$_2$ presents another major concern. Therefore, a transition to a gate material with a higher dielectric constant is critical for further CMOS scaling. A number of high-K dielectrics, such as Ta$_2$O$_5$ [1], Al$_2$O$_3$ [2], Laj$_2$O$_3$ [2], ZrO$_2$ [3], HfO$_2$ [4], and several silicon nitrides have been proposed to replace SiO$_2$ in the gate stack. Stability of these materials in contact with silicon during high-temperature processing steps remains a major problem. Therefore, it might be a few years before a successful integration of a high-K dielectric into CMOS fabrication process becomes reality. At the same time, Si$_3$N$_4$, which has a relatively high dielectric constant of 7.5 (almost twice that of SiO$_2$), has been used by the semiconductor industry for decades and is relatively easy to integrate into the fabrication process. Good performance of Si$_3$N$_4$ transistors has already been demonstrated [5], [6]. However, it is necessary to demonstrate good reliability of thin Si$_3$N$_4$ before it can replace SiO$_2$ as gate dielectric. Studies of time-dependent dielectric breakdown [5], [7] and time-dependent dielectric wearout [8] indicate that Si$_3$N$_4$ under Fowler–Nordheim stress meets reliability requirements. It still remains to be shown that hot-carrier reliability of Si$_3$N$_4$ gate dielectrics is acceptable. Earlier work [7] indicates good hot-carrier reliability of nMOSFET Jet Vapor Deposition (JVD) nitride transistors with 31 Å equivalent oxide thickness. In this paper, we will show that the hot-carrier lifetime of Si$_3$N$_4$ pMOSFETs is similar to that of SiO$_2$ pMOSFETs.

We also examine the mechanism responsible for pMOSFET degradation. It has been long known that the mechanism responsible for the device degradation in nMOSFET is interface-state generation. The situation for pMOSFETs is less clear. It had long been believed that hot-carrier reliability of pMOSFETs is not as serious an issue as hot-carrier reliability of nMOSFETs for the following reason. The mean free path of holes in silicon is about one half that of the electrons [9]; therefore, holes scatter more frequently and fewer of them reach high enough energies (about 4 eV) to create interface states [10]. However, as the transistor channel length has been scaled down into the deep-submicron regime (and supply voltages have been reduced) hot-carrier induced degradation of pMOSFETs has been approaching that of nMOSFETs [11]. Consequently, the hot-carrier reliability of pMOSFETs has been studied in more detail. Three hot-carrier degradation mechanisms in pMOSFETs have been identified [12], [13]. The first is negative oxide charge trapping. Electron trapping near the drain region leads to a reduction in the threshold voltage and to the effective channel shortening. As a result, pMOSFET drive current increases. This mechanism is most important in longer channel pMOSFETs, and gate current $I_{GS}$ has been used as a predictor of the device lifetime. The second mechanism is the generation of interface states by hot holes, which leads to channel mobility degradation. In this case, the substrate current $I_{SUB}$ should be used to predict the device lifetime, and the third mechanism is positive oxide charge trapping. Interface-state generation has been shown to be the dominant degradation mechanism for 0.25-μm surface channel pMOSFETs [12]. We will show that this conclusion remains true for our 100-nm devices, for both oxide and nitride gate dielectrics.

II. DEVICE FABRICATION AND CHARACTERIZATION

A. Fabrication Stage

The Si$_3$N$_4$ transistors with 100-nm channel length were made using a LOCOS-isolation CMOS process without halo implant. The silicon–nitride gate dielectric was deposited by Jet Vapor Deposition (JVD) [14] at Yale University. Following a 5-min 800 °C anneal in N$_2$, undoped poly-Si was deposited by LPCVD. $I_{IL}$-line lithography and photoresist ashing in O$_2$.
plasma were used to define gate electrodes down to 100 nm. Following the gate patterning, source and drain regions were formed by ion implantation. A dose $1 \times 10^{14} \text{ cm}^{-2}$ B$^{+}$ was used to form the source and drain extensions in pMOSFETs. Dopants were activated by rapid thermal annealing in N$_2$. The SiO$_2$ transistors used in this study for comparison purposes were fabricated using a similar process.

### B. Characterization

The gate-dielectric equivalent oxide thickness $t_{eq}$ is extracted using a quantum mechanical simulator [15]. The quantum mechanical simulator solves Poisson’s and Schrödinger’s equations self-consistently in order to determine the precise inversion/accumulation charge distribution in the substrate at various gate bias conditions. This charge distribution is then used to produce a simulated capacitance versus voltage characteristic. The values of the oxide-equivalent dielectric thickness and the substrate doping concentration are varied until a good match to the experimental data is achieved. The simulator also considers the voltage drop in the polysilicon gate electrode in order to account for the polysilicon depletion effect (the decrease in the gate capacitance in the strong inversion regime.) For the nitride transistors, $t_{eq}$ is 14 Å and n-well doping concentration is $4 \times 10^{14} \text{ cm}^{-3}$ (Fig. 1). For the oxide transistors, $t_{eq}$ is 16 Å and n-well doping concentration is $7 \times 10^{17} \text{ cm}^{-3}$.

Fig. 2 shows the output current characteristics for both types of transistors. At low drain bias, the oxide transistor has a higher drain current. This is due to the well-known fact that nitride transistors have lower channel mobility. At high drain bias (close to the supply voltage), the situation is reversed, and the nitride transistor has a higher current drive. This higher current drive can be explained by higher inversion charge density in 14 Å Si$_3$N$_4$ transistors. The major advantage of the Si$_3$N$_4$ gate dielectric is the reduction of the gate leakage current (Fig. 3). The leakage current of the 14 Å Si$_3$N$_4$ pMOSFET is an order of magnitude lower than that of the 16-Å SiO$_2$ pMOSFET. The reduction in the gate leakage current for nMOSFETs is even larger [16].

### III. Device Fabrication and Characterization

The drain voltage $V_D$ during the hot carrier stress ranged from $-4.5$ to $-6.5$ V; the gate voltage $V_G$ was chosen to maximize the substrate current. The exact stress conditions for each of the nitride transistors are listed in Table I. As we have outlined in the introduction, hot-electron injection becomes a relatively less important mechanism of pMOSFET degradation as the channel length becomes shorter than 0.25 μm [12], [13], [17]. Therefore, we do not expect the stress at low $V_G$ ($V_G \approx V_D/5$), which favors hot-electron injection, to be the worst-case stress condition. Many recent papers were dedicated to the discussion of whether stress at maximum gate voltage ($V_G = V_D$) or stress at maximum substrate current $I_{Sub}$ leads to the fastest device degradation [17], [18]. We chose to use

<table>
<thead>
<tr>
<th>Drain voltage $V_D$ (V)</th>
<th>Gate voltage $V_G$ (V)</th>
<th>Peak $I_{Sub}$ (μA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-4.5</td>
<td>-1.2</td>
<td>0.16</td>
</tr>
<tr>
<td>-5.0</td>
<td>-1.4</td>
<td>0.5</td>
</tr>
<tr>
<td>-5.3</td>
<td>-1.5</td>
<td>1.0</td>
</tr>
<tr>
<td>-5.5</td>
<td>-1.6</td>
<td>2.0</td>
</tr>
<tr>
<td>-5.6</td>
<td>-1.5</td>
<td>2.4</td>
</tr>
<tr>
<td>-6.5</td>
<td>-2.0</td>
<td>3.6</td>
</tr>
</tbody>
</table>
Fig. 4. Degradation in (a) transconductance and (b) gate leakage current as a result of hot-carrier stress. (Stress $V_D = -6.5 \, \text{V}$, stress time $= 500 \, \text{s}$).

IV. RESULTS AND DISCUSSION

A. Hot-Carrier Degradation Mechanism

We examine the mechanism responsible for the device degradation by examining the change in the threshold voltage (Fig. 6). In the early stages of stress, electrons are trapped in the gate dielectrics as indicated by the positive $\Delta V_T$. Electron trapping follows a “logarithmic” dependence on time [12]. This is consistent with a model in which the electrons are created by impact ionization near the drain region, propelled toward the gate electrode by the vertical electric field, and captured by the traps which exist in the dielectric. Silicon nitride is known to have a higher density of traps than silicon oxide; in addition, its physical thickness is almost twice that of the oxide, hence, silicon nitride shows a larger positive $\Delta V_T$. In the later stages of stress, $\Delta V_T$ becomes negative indicating a positive charge buildup in the gate dielectric. The positive charge can result from either hole trapping in the dielectric or the creation of positively charged interface states at the dielectric interface. In practice, it may be hard to draw a distinction between the two phenomena, as it is hard to distinguish between bulk and interface traps in the case of ultrathin dielectrics. We believe that interface state generation is predominant, as the electric field near the drain does not favor hole injection in the dielectric. Furthermore, the change in $V_T$ becomes a power-law function of time, consistent with the interface generation model [12].
To further support the interface-state generation model, we note that the result of the charge trapping alone on device performance is quite modest. A $2 \times 10^4$-s stress at $V_D = -5.5$ V leads to a $-40$-mV shift in $V_T$; this would translate approximately into a 3% change in $I_D$. In reality, however, drain current changes by more than 10% during this stress. Essentially, all of the degradation in $I_D$ is due to the decrease in hole mobility. Therefore, interface-state generation is the dominant degradation mechanism.

B. Lifetime Comparison Between Si$_3$N$_4$ and SiO$_2$ Devices

Our next task is to determine the reliability properties of gate nitride as expressed by the hot-carrier lifetime. In general, hot-carrier lifetime depends on the properties of the gate dielectric as well as on LDD design. Thus, simply determining the lifetime of transistors with a new gate dielectric is rather meaningless. Instead, the lifetime of the Si$_3$N$_4$ devices should be compared to the lifetime of SiO$_2$ devices with a similar LDD design. We verified that our nitride and oxide transistors are indeed comparable in terms of source–drain engineering by comparing the substrate currents in these devices. Substrate current is an exponential function of the peak electric field in the channel pinch-off region [19]. Since both device types have the same peak $I_{SUB}$ as a function of drain voltage (Fig. 7), the electric field in the pinch-off region is the same for these two device types at a given $V_D$. Therefore, we can directly compare the lifetime of the Si$_3$N$_4$ transistors against the lifetime of the control SiO$_2$ devices. Also included in Fig. 7 is the substrate current measured for SiO$_2$ devices with a more aggressive (higher doping) LDD design. At a given $V_D$, these devices have a higher peak electric field, and therefore a higher $I_{SUB}$. Lower lifetime for these devices should be expected at a given $V_D$. One still should be able to compare the lifetimes of different dielectrics if the comparison is made at the same $I_{SUB}$. (We have already confirmed that interface-state generation by hot holes is the major degradation mechanism; therefore, $I_{SUB}$ is the correct lifetime predictor.) Fig. 8 shows that the lifetime follows the same power-law dependence on $I_{SUB}$ with the slope of 1.5 commonly observed for pMOSFETs [10], [20] for the devices with different gate dielectrics and different LDD designs.

V. SUMMARY AND CONCLUSION

We have found that the hot-carrier lifetime of pMOSFETs with JVD nitride gate dielectric is similar to that of devices with SiO$_2$ gate dielectric. This conclusion is in agreement with the observation by other researchers [21] that interface generation in oxide and oxynitride pMOSFETs is insensitive to nitridation. The reason behind this insensitivity is likely to be the fact that hot carriers cause damage to the silicon surface [19]. We have also confirmed that interface-state generation remains the dominant device degradation mechanism for deep-submicron pMOSFETs. Therefore, $I_{SUB}$ should be used as the predictor of device lifetime.

The lifetime of transistors as a function of $1/V_D$ is shown in Fig. 9. The extrapolation to low operating voltages indicates that a supply voltage of around 3.8 V would lead to a 10-year lifetime for both Si$_3$N$_4$ and control SiO$_2$ transistors. This high voltage is explained by the conservative LDD design in our devices. A more aggressive LDD design would lead to a 2.2-V supply voltage limit, while improving the transistors’ current drive.

In conclusion, we have shown that hot-carrier reliability of Si$_3$N$_4$ transistors is no worse than that of SiO$_2$ transistors. In addition, a 14-Å Si$_3$N$_4$ pMOSFET has higher $I_{DSAT}$ and lower gate leakage current than a 16-Å SiO$_2$ pMOSFET. This makes Si$_3$N$_4$ a promising alternative to SiO$_2$ as the dielectric of choice for future generations of CMOS devices.
ACKNOWLEDGMENT

Device fabrication was done in the Microfabrication Laboratory of the University of California at Berkeley. JVd nitride was deposited at Yale University.

REFERENCES


Igor Polischuk (S’98) received the B.Sc. degree in physics from the California Institute of Technology, Pasadena, in 1997 and a M.S. degree in electrical engineering from the University of California, Berkeley, in 1999. He is currently working toward the Ph.D. degree at the University of California, Berkeley. His research interests include reliability of ultrathin gate oxides and high-K dielectrics, metal gate technology, and carrier transport modeling in MOS devices.

Mr. Polischuk received the California Fellowship in Microelectronics in 1997 and currently holds the SRC/NIST Graduate Fellowship.

Yee-Chia Yeo (S’98) received the B.Eng. degree with first class honors and the M.Eng. degree from the National University of Singapore (NUS), both in electrical engineering. He is currently working toward the Ph.D. degree in electrical engineering at the University of California, Berkeley.

He has worked on the characterization of lasers for low-cost optoelectronics at the British Telecommunications Laboratories, Ipswich, U.K., and also on the study of GaN-based quantum-well lasers at NUS. His research interests include MOS device physics, sub-100-nm device fabrication, strained SiGe-channel MOSFETs, metal gates, and advanced gate dielectrics.

Mr. Yeo was awarded the 1995 IEEE Prize, the 1996 Lee Kuan Yew Gold Medal, and the 1996 Institution of Engineers, Singapore (IES) Gold Medal for being the best undergraduate in electrical engineering at NUS. He is also the recipient of the 1997–2002 Overseas Graduate Scholarship from NUS.

Qiang Lu (S’01) received the B.S. degree in physics from Peking University, China, in 1996. He is currently a graduate student in the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley.

His research interests include high-K dielectrics and metal gate materials for MOS devices, and oxide reliability.

Tsu-Jae King (M’91) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA.

At Stanford, her research involved the seminal study of polycrystalline silicon–germanium films and their applications in metal–oxide–semiconductor (MOS) technologies. She joined the Xerox Palo Alto Research Center, Palo Alto, CA, as a Member of Research Staff in 1992 to research and develop polycrystalline–silicon thin-film transistor technologies for high-performance display and imaging applications. She joined the faculty of the University of California, Berkeley, in August 1996 where she is currently an Associate Professor of Electrical Engineering and Computer Sciences, and the Faculty Director of the UC Berkeley Microfabrication Laboratory. Her research activities are in sub-100-nm MOS devices and technology, and thin-film materials and devices for integrated microsystems and large-area electronics. She has authored or co-authored over 150 papers and holds five U.S. patents.

Cheming Hu (S’71–M’76–SM’83–F’90) received his B.S. degree from the National Taiwan University in 1968 and the M.S. and Ph.D. degrees from the University of California, Berkeley.

He is the TSMC Distinguished Professor of Electrical Engineering and Computer Sciences at UC Berkeley. His research areas include microelectronic devices and technology and device modeling for circuit simulation. He has authored or co-authored over 500 research papers.

He is a member of the National Academy of Engineering, a fellow of the Institute of Physics, and an honorary professor of the Chinese Academy of Science, Beijing, and Chiao Tung University, Taiwan. He leads the development of the MOSFET model BSIM, the industry standard model for IC simulation. He received the 1997 Jack A. Morton Award for contributions to MOSFET reliability. He has received UC Berkeley’s highest honor for teaching—the Distinguished Teaching Award, and the DARPA Most Significant Technological Accomplishment Award for co-developing the FinFET transistor structure.