Charge-Trap Memory Device Fabricated by Oxidation of $\text{Si}_{1-x}\text{Ge}_x$

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Abstract—In this work, we describe a novel technique of fabricating germanium nanocrystal quasinonvolatile memory device. The device consists of a metal-oxide-semiconductor field-effect transistor (MOSFET) with Ge charge-traps embedded within the gate dielectric. The trap formation method provides for precise control of the thicknesses of the top (control) and bottom (tunneling) oxide layers which sandwich the charge-traps, via thermal oxidation. This memory device exhibits write/erase speed/voltage and retention time superior to previously reported nano-crystal or charge-trap memory devices. A detailed description of the novel process for fabricating the Ge charge-trap MOS memory is given, along with the resultant memory-cell performance characteristics.

Index Terms—Charge-trap memory, Ge nano-crystal.

I. INTRODUCTION

The demands of more powerful portable electronics and embedded systems heighten the need for low-power high-density memory in the future. The state-of-art high-density semiconductor memories are DRAM and flash. DRAM cell allows fast write and erase, in the range of 100 ns or less [1]. However, its data retention time is limited by junction and transistor leakage to less than a few seconds [2]. As a result, frequent refresh is required, which increases the power consumption of the memory array even with no change in its data content. The need for large storage capacitor in every DRAM cell makes it impossible to form high-density memory cell without complex cell structure and/or new dielectric materials [3], [4]. Flash memory cells designed for ten years of data retention requiring the use of relatively thick tunnel oxide that greatly compromise both its write and erase speed and endurance [5], [6].

It is well known that oxide tunneling current increases rapidly as the oxide thickness is reduced to below 35 Å, where the direct tunneling current mechanism dominates. Oxide reliability (charge-to-breakdown) has been found to improve dramatically also, due to minimal oxide damage by direct tunneling [7], [8]. These attributes of the very thin oxide suggest the possibility of fast write/erase speed and high endurance for a memory cell. However, significant charge leakage due to direct tunneling current at quiescent gate voltage shortens the data-retention time dramatically; this makes floating gate memory device with a very thin tunnel oxide unattractive. One way to increase the retention time is to replace the floating gate with a silicon nitride layer for charge trapping [13].

Recently, a single-transistor memory-cell structure with nano-crystal charge-storage sites embedded within the gate dielectric has been proposed and demonstrated [11]. By using electrically isolated charge-storage nodules in the oxide, charge leakage through localized oxide defects is greatly reduced; hence, a much thinner tunneling oxide (for faster write/erase speed) can be employed. The possibility of the charge-storage memory device which exceeds the performance limits of a conventional floating-gate device has attracted a great deal of interest and is spurring rapid progress in this area [9], [10]. Quasinonvolatile MOS memory devices employing silicon, germanium or tin nanocrystal charge-storage sites produced by ion implantation into the gate oxide have been demonstrated in recent studies [11], [12]. These nanocrystal memory devices fabricated by ion implantation exhibited superior data-retention characteristics than that of the conventional floating-gate devices. Limitations of the ion implantation technique place a lower limit on the gate oxide thickness. In addition, ion implantation may compromise the integrity of the oxides.

In this work, we describe a new, novel technique for creating germanium charge-trap sites within the gate dielectric of a MOSFET. The control oxide, charge-trap sites, and the tunneling oxide are formed through a sequence of thermal oxidation of $\text{Si}_{1-x}\text{Ge}_x$ at various temperatures. The resulting memory device exhibits fast WRITE/ERASE speed, long data retention time and superior endurance with nondestructive read. The process of forming this memory cell is compatible to the typical CMOS process, therefore can be easily adapted in the fabrication of embedded circuits.

II. PROCESS FLOW

The schematic cross-section of a new charge-trap-based quasinonvolatile memory device is shown in Fig. 1. The single-transistor memory structure can be fabricated using conventional wafer-processing techniques. A novel method of forming the gate-dielectric stack (consisting of a upper layer of control oxide, a middle oxide layer with embedded germanium nano-crystals and a lower layer of tunneling oxide) is illustrated in Fig. 2. This technique provides excellent thickness control for the top and bottom oxide layers that sandwich the nano-crystals. A thin epitaxial layer of $\text{Si}_{1-x}\text{Ge}_x$ is first formed on the surface of a Si wafer by ion implantation and subsequent high-temperature wet oxidation, which causes the implanted Ge atoms to pile up at the Si/SiO$_2$ interface. The
Ge segregates out of the growing oxide under these oxidation conditions [14]. After the high temperature oxide film is etched off, the control oxide layer is grown at 800 °C in dry O₂. Under these conditions, Ge is not incorporated into the oxide, and thus SiO₂ is grown. Next, a Si₁₋ₓGeₓO₂ layer is grown at 650 °C in a wet ambient [15] in order to incorporate the Ge into the gate dielectric stack. Next, the tunneling oxide is grown at 800 °C in dry O₂. Finally a high temperature (900 °C) anneal step is employed to cause the Ge within the oxide to precipitate and form nanocrystals. A cross-sectional transmission electron micrograph of a gate-dielectric stack formed by this new technique is shown in Fig. 3. Ge nanocrystals of size ranging from 50 to 100 Å in diameter are seen in this sample, which was fabricated with a relatively high Ge implant dose. Memory devices were fabricated with lower Ge implant doses, in order to form smaller Ge nanocrystals that are more compatible with thin dielectric stacks. The size to the Ge nanocrystals in the fabricated devices is estimated to be less than 25 Å. A small amount of Ge remains at the Si/SiO₂ interface, creating interface traps and thereby degrading the transistor performance [16]. Nitrogen implantation followed by high-temperature annealing was employed to passivate the Ge. This significantly improved the transistor’s capacitance–voltage (C–V) and current–voltage (I–V) characteristics.

III. MEMORY DEVICE CHARACTERISTICS

The subthreshold characteristics of the Ge nanocrystal memory device are shown in Fig. 4. It is found that the transistor threshold voltage shifts 0.4 V after a +4 V, 100 ns-write pulse. The threshold-voltage shift, \( \Delta V_t \), is given by the following expression:

\[
\Delta V_t = \frac{d}{\varepsilon_{os}} Q_t
\]

where \( d \) is the distance between the trapped charge and the gate electrode, and \( Q_t \) is the areal density of trapped charge (residing on the Ge nanocrystals) in the gate dielectric. Using \( d = 30 \) Å, \( \Delta V_t = 0.4 \) V, the number of electrons trapped in the Ge nanocrystals was estimated to be \( 3.5 \times 10^{12} \) cm⁻². Due to the Coulomb blockade effect, only one electron can be trapped in each Ge nanocrystals. Hence, the size of the nanocrystal was estimated to be about 20 Å in diameter with center to center spacing of 50 Å.

The programming characteristics of the nanocrystal memory device are shown in Fig. 5 for several write/erase voltages. \( \Delta V_t \) saturates as the write time increases and also as the write voltage increases. This is because there is a finite number of the charge-storage sites provided by the Ge nanocrystals. The device shows symmetrical write and erase characteristics. The erase time of less than 50 ns is the fastest speed ever reported for a nanocrystal memory device.

The endurance of the Ge nanocrystals memory device cell is tested using +4 V/–4 V write and erase cycles with 100 ns...
pulse width. As Fig. 6 shows, endurance is found to be better than $10^9$ write/erase cycles, with negligible degradation in transistor current-versus-voltage characteristics. The data-retention characteristics at both the room temperature and 85°C of the device after $10^9$ write/erase cycles are shown in Fig. 7. Less than 5% reduction in the threshold voltage window was observed after $10^3$ s. This memory device has a data-retention longer than one day at room temperature and about 1 h at 85°C.

**IV. DISTRIBUTION OF THE PROGRAMMED STATES**

In order to serve in a large-scale memory array, the distribution of the threshold voltages of the memory cells must be investigated. The threshold voltage variation in the erased or uncharged state can be controlled with the usual production disciplines. The threshold voltage variation in the programmed or charged state warrants additional studies due to the inherited properties of the Ge nanocrystals formed by the proposed method. The threshold voltages across the wafer were measured both in the erased and the programmed states. For high-density memory application, the memory devices have to be scaled to deep submicron size. The variation in the number of electrons captured, i.e., the number of nanocrystals in the memory cell, has to be within a certain tolerance determined by the design of the sense amplifier. The threshold voltage difference between the programmed and erased states of 30 memory cells with sizes of 100, 10, 1, 2 $\mu$m$^2$, respectively, were measured and shown in the box plot in Fig. 8. It is found that the variation of the threshold voltage at the programmed states increases, as the size of the transistor becomes smaller. The histograms in Fig. 9 further examine the variation of the nanocrystals in these memory devices.
Due the nonuniformity of the size and density of the germanium nanocrystals, the variation of the threshold voltage in the programmed states increases as the size the memory cell decreases. This results suggests that the uniformity of the size and density of the nanocrystals must be well controlled for application in high density and large-scale memory arrays.

V. CONCLUSION

A novel technique of fabricating Ge nanocrystal quasinonvolatile memory devices has been developed. It has excellent flexibility in oxide thickness control and has produced devices with write speed/voltage and retention time superior to previous nanocrystal devices. This fast write/erase quasinonvolatile device is potentially useful in low power, high-density memory products. It is also a candidate for embedded memory application since its fabrication process is very compatible with logic CMOS processes.

REFERENCES


Ya-Chin King (S’92–M’99) was born in Taiwan, R.O.C. She received the B.S. degree in electrical engineering from National Taiwan University, Taipei, in 1992, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 1994 and 1999, respectively. Her dissertation was on thin oxide technology and novel quasinonvolatile memory. She joined National Tsing-Hua University, Hsinchu, Taiwan, in August 1999 as an Assistant Professor. Her research topics include: thin gate dielectric, CMOS image sensor and nonvolatile memory design.
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Dr. Hu is a member of the U.S. National Academy of Engineering and a Life Honorary Professor of the Chinese Academy of Science. In 1991, he received the Excellence in Design Award from Design News and the inaugural Semiconductor Research Corporation Technical Excellence Award for leading the research of IC reliability simulator, BERT. He received the SRC Outstanding Inventor Award in 1993 and 1994. He leads the development of the MOSFET model BSIM3v3 that has been chosen as the first industry standard model for IC simulation by the Electronics Industry Alliance Compact Model Council and given an R&D 100 Award in 1996 as one of the 100 most technologically significant new products of the year. The IEEE awarded him the 1997 Jack A. Morton Award for his contributions to the physics and modeling of MOSFET reliability. Also in 1997, he received UC Berkeley’s highest honor for teaching – the Distinguished Teaching Award. In 1998, he received the Monie A. Ferst Award of Sigma Xi for encouragement of research through education. He received the Pan Wen Yuan Foundation Award for outstanding research in electronics in 1999.