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MOS Capacitance Measurements for High-Leakage Thin Dielectrics

Kevin J. Yang and Chenming Hu

***Abstract*—As oxide thickness is reduced below 2.5 nm in MOS devices, both series and shunt parasitic resistances become significant in capacitance–voltage ($C-V$) measurements. A new technique is presented which allows the frequency-independent device capacitance to be accurately extracted from impedance measurements at two frequencies. This technique is demonstrated for a 1.7 nm SiO_2 capacitor.**

***Index Terms*—Capacitance measurement, MIS devices.**

I. Introduction

Capacitance–voltage ($C-V$) measurements are a fundamental characterization technique for MOS devices. Accurate determination of device capacitance is critical for oxide thickness extraction [1], metallurgical channel length determination [2], mobility measurement [3] and interface trap characterization [4].

MOS technology scaling is rapidly driving the gate oxide thickness to below 2 nm [5]. As oxide thickness is reduced, the direct tunneling leakage current increases exponentially [1]. As a result, the quasistatic capacitance measurement becomes difficult. The leakage problem may be overcome by measuring the capacitance at a very high frequency so that the capacitive current is dominant. At very high frequency, however, the series resistance becomes significant because of the low impedance of the capacitor. Hence, one must account for the simultaneous presence of both the series and shunt parasitic resistances in the capacitance-voltage measurement. The true capacitance can be determined from measurements made at two different frequencies [6]. This work demonstrates a method to measure a MOS capacitor with thin gate oxide and large tunneling current.

II. Theory

The three-element circuit model of a MOS capacitor with leaky gate oxide is shown in Fig. 1(a). C represents the actual frequency-independent device capacitance, R_p represents the effective device resistance due to leakage (tunneling) through the oxide, and R_s represents the series resistance of the substrate and the gate. From a single measurement of impedance phase and magnitude, however, only two of these three parameters may be ascertained.

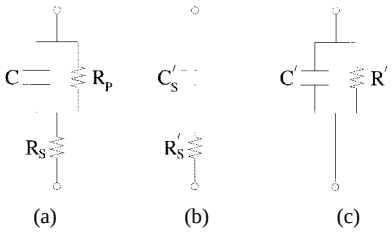

Fig. 1. Small-signal equivalent circuit models of MIS capacitor: (a) accurate model, (b) series circuit model for low-leakage devices, and (c) parallel circuit model for low series resistance devices.

For gate oxides thicker than 3 nm, the tunneling current is small and the device is dominated by series resistance. In this case, the device capacitance may be found from a single measurement by neglecting the shunt resistance and determining the capacitance using the series circuit model in Fig. 1(b).

$C-V$ measurements of very thin oxides with large leakage currents are often performed using the parallel circuit model in Fig. 1(c), which neglects series resistance. As shown in Fig. 2, the measured capacitance using the parallel circuit model is dependent on frequency for a MOS capacitor with gate oxide thickness (optical) of 1.7 nm. Furthermore, the magnitude of the capacitance decreases as bias increases due to increasing tunneling current.

It will be demonstrated that this frequency-dependent roll-off can be eliminated by returning to the three-element circuit model, which includes series resistance.

The impedance of the three-element circuit model shown in Fig. 1(a) is given by

$$Z = R_s + \frac{R_p(1 - j\omega C R_p)}{1 + \omega^2 C^2 R_p^2}. \tag{1}$$

The impedance of the parallel circuit model in Fig. 1(c) is given by

$$Z = \frac{D' - j}{\omega C'(1 + D'^2)} \tag{2}$$

where $D' = \frac{1}{\omega R' C'}$ is the dissipation, and R' and C' refer to measured values.

Equating the imaginary parts of the measured impedance (2) and the true impedance (1), one obtains

$$\frac{1 + \omega^2 C^2 R_p^2}{C R_p^2} = \omega^2 C'(1 + D'^2). \tag{3}$$

Measuring the capacitance and dissipation at two different frequencies, substituting into (3) for each frequency, subtracting, and solving for C, one obtains

$$C = \frac{f_1^2 C_1'\left(1 + D_1'^2\right) - f_2^2 C_2'\left(1 + D_2'^2\right)}{f_1^2 - f_2^2} \tag{4}$$

where C_1' and D_1' refer to the values measured at the frequency f_1 and C_2' and D_2' refer to the values measured at the frequency f_2.

Proceeding in a similar manner with the real parts of the impedance, one obtains the relations for the parasitic series and shunt

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The authors are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA.

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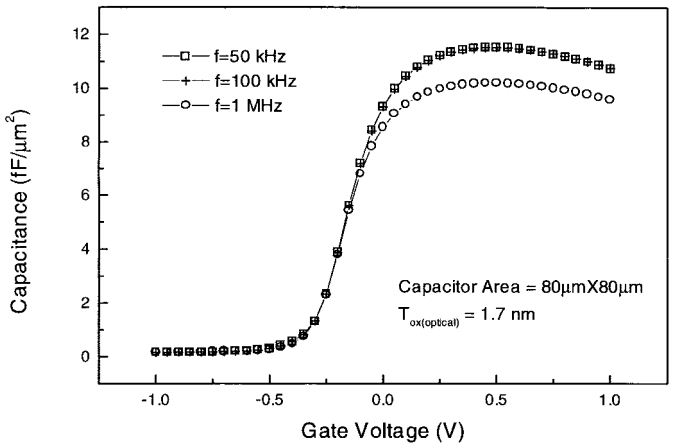

Fig. 2. High-frequency $C-V$ measurement of MOS capacitor at 50 kHz (square), 100 kHz (cross), and 1 MHz (circle). $C-V$ characteristics depend on frequency in the parallel circuit model.

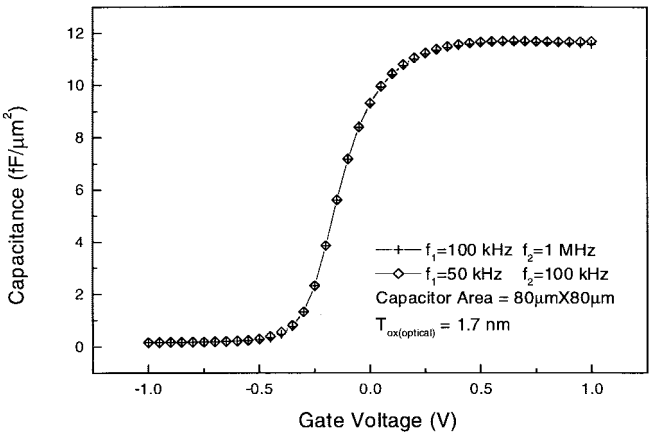

Fig. 3. $C-V$ data measured with the new technique obtained by combining raw data from 100 kHz and 1 MHz (cross) and 50 kHz and 100 kHz (diamond).

resistances

$$R_p = \frac{1}{\sqrt{\omega^2 C'C'(1+D'^2) - \omega^2 C'^2}} \tag{5}$$

and

$$R_s = \frac{D'}{\omega C'(1+D'^2)} - \frac{R_p}{1+\omega^2 C'^2 R_p^2}. \tag{6}$$

III. Measurement

A MOS capacitor was fabricated using *in situ* doped n^+-polysilicon gate on n-type silicon substrate with resistivity of 10–20 Ω-cm. Capacitance C' and dissipation D' of a MOS capacitor with 1.7 nm (optical) gate oxide were measured using the parallel circuit model at 100 kHz and 1 MHz using an HP4284A (see Fig. 2). Fig. 3 shows the frequency-independent device capacitance obtained from (4) using both qualitatively similar (50 kHz and 100 kHz) and dissimilar (100 kHz and 1 MHz) measured data.

IV. Conclusion

A technique has been developed for extracting the frequency-independent capacitance and thickness of thin dielectrics from high-frequency $C-V$ measurements performed at two different frequencies. This technique can be integrated easily into a routine $C-V$ measurement procedure and has been demonstrated to be suitable for obtaining accurate $C-V$ characteristics of a MOS capacitor with 1.7 nm thick gate oxide.

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