Channel Width Dependence of Hot-Carrier Induced Degradation in Shallow Trench Isolated PMOSFET’s

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Abstract—Channel width dependence of the hot-carrier induced degradation in pMOSFET’s with shallow trench isolation structure is investigated. Enhanced degradation is observed in narrow channel width device. The narrow width device shows large electron trapping efficiency of the gate oxide film though the gate current is smaller than the wide width device. Mechanical stress caused by shallow trench isolation may be responsible for this phenomenon.

Index Terms—Hot-carrier reliability, mechanical stress, trench isolation.

I. INTRODUCTION

SHALLOW trench isolation (STI) is now widely used in memory and logic products. Trench isolation can produce narrow device width. The narrow width MOSFET’s are commonly used in SRAM and DRAM cells and also peripheral circuits, such as clocked inverter used in high speed synchronous SRAM which duty cycle is pretty high and affect circuit performance.

Although the STI can achieve narrow device width, most of the device evaluation such as hot-carrier reliability are performed by using wide width device, e.g., W = 10 or 20 μm. Several studies have been reported on the enhanced hot-carrier induced degradation for narrow width n- and pMOSFET’s with LOCOS isolation [1]–[3]. Recently, Nishigohri et al. have reported that narrow width device exhibits significantly worse hot-carrier reliability for nMOSFET’s with STI structure [4]. There has been, however, no report on the hot-carrier reliability of narrow width pMOSFET with STI structure.

Generally, the gate length of the memory cell is longer than that of the peripheral circuit. In case of high speed SRAM with 0.35 μm design for example, the gate length \( L = 0.3 \mu m \) \((W > 10 \mu m)\) is used for peripheral circuit and \( L = 0.35 \mu m \) \((W = 0.35 \mu m)\) is used for the memory cell. The MOSFET with shorter gate length shows shorter lifetime under the same channel width. Therefore, it seems reasonable to use \( W/L = 20 \mu m/0.3 \mu m \) MOSFET to evaluate hot-carrier reliability for 0.35 μm high speed SRAM. However, there is no guarantee that the \( W/L = 0.35 \mu m/0.35 \mu m \) device shows longer lifetime than \( W/L = 20 \mu m/0.3 \mu m \) device.

Fig. 1. Initial \( I_d-V_g \) characteristics of both \( W = 0.35 \mu m \) and \( W = 20 \mu m \) pMOSFET’s with substrate bias \( V_s = 1 \) V. No kink characteristics related to the corner device were observed in subthreshold region by optimized trench process.

Consequently, it is important to study the hot-carrier reliability in narrow width region.

In this paper, channel width dependence of the hot-carrier reliability of pMOSFET with STI structure is presented. Accelerated dc stress is performed under several gate voltage \((V_g)\), which include the maximum gate current \((I_{G_{max}})\) condition. The hot-carrier stress time dependence of the gate current \((I_g)\) and electron trapping efficiency of the gate oxide film are analyzed to explain the experimental results. A possible mechanism that accounts for the experimental results is also suggested.

II. EXPERIMENTS

The pMOSFET’s used in this experiment were fabricated by 0.35 μm dual gate CMOS process [5]. The trench was filled by TEOS-O₂ film and 1200 °C annealing was carried out after CMP planarization. The gate oxide film thickness was 6 nm and the gate electrode consisted of SiN (200 nm)/WSi₂ (100 nm)/poly-Si (200 nm) stacked structure with 70 nm SiN sidewall. The gate poly-Si was doped by boron implantation at an energy of 15 keV with a dose of \( 3 \times 10^{15} \) cm\(^{-2}\). The LDD region was fabricated by BF₂ implantation at an energy of 20 keV with a dose of \( 1 \times 10^{14} \) cm\(^{-2}\).

Since the trench edge was optimized [5], both wide and narrow channel width pMOSFET’s exhibited no kink characteristics in the subthreshold region even with the substrate bias as shown in Fig. 1. In order to investigate the channel width dependence of the hot-carrier induced degradation, several...
channel width pMOSFET's such as \( W = 0.35 \), 1, and 20 \( \mu m \) were evaluated. The gate length of the measured device was \( L = 0.35 \) \( \mu m \) and saturation drain current \( (I_{d_{sat}}) \) at \( V_g = V_d = -3.3 \) V condition and threshold voltage \( V_{th} \) shift were used as a degradation monitor. The hot-carrier stress conditions for each device were \( V_d = -4.6 \) V and \( V_g \) varied from \(-0.3\) to \(-1.5\) V, which includes the maximum gate current \( (I_{g_{max}}) \) condition. The hot-carrier stress tests were interrupted periodically to measure the \( I_{d_{sat}} \) degradation \( (\Delta I_{d_{sat}}/I_{d_{sat}}) \) and the threshold voltage shift \( (\Delta V_{th}) \). Constant current stress was also applied to evaluate the gate oxide film quality for both \( W = 20 \) \( \mu m \) and \( W = 0.35 \) \( \mu m \) pMOSFET’s. Two-dimensional (2-D) device simulation was also carried out to clarify the degradation mechanism.

III. RESULTS AND DISCUSSION

A. Hot-Carrier Stress Results

The channel width dependence of the drain current degradation \( \Delta I_{d_{sat}}/I_{d_{sat}} \) is shown in Fig. 2 as a parameter of hot-carrier stress time. The hot-carrier stress condition is \( V_g = I_{g_{max}} \) at \( V_d = -4.6 \) V and the gate length is \( L = 0.35 \) \( \mu m \). As the channel width becomes narrower, \( \Delta I_{d_{sat}}/I_{d_{sat}} \) becomes larger. For each stress time, \( \Delta I_{d_{sat}}/I_{d_{sat}} \), values of \( W = 0.35 \) \( \mu m \) device are from three to five times larger than those of \( W = 20 \) \( \mu m \) device.

Fig. 3 shows \( I_d-V_g \) characteristics for both \( W = 20 \) \( \mu m \) and \( W = 0.35 \) \( \mu m \) pMOSFET’s after fifty minutes hot-carrier stress. Initial characteristics are also indicated in the same figure. After the hot-carrier stress, the threshold voltage of both devices become lower. This means that degradation is caused by the trapped electrons [6] into the gate oxide film. The subthreshold slope does not change after the hot-carrier stress. This is because the interface states are shielded by the negative charge [7], [8].

No kink characteristics are also observed in the subthreshold region after the hot-carrier stress for both devices. If the corner portion of the channel degrades faster than the center of the channel, kink characteristics will appear in the subthreshold region [9]. However, our measurement results present no kink characteristics. The reason is considered as follows. The wide transistor can be divided into two devices, such as center and corner transistor. As shown in the Fig. 1, the current–voltage \( (I-V) \) characteristics of the corner transistor corresponds to that of \( W = 0.35 \) \( \mu m \) device. The \( x \)-axis is normalized to \( V_{th} \) and the difference in \( I_d \) at certain \( V_g \)–\( V_{th} \) corresponds to the difference in \( W \) (approximately 60).

The \( I-V \) characteristics of \( W = 20 \) \( \mu m \) device includes that of \( W = 0.35 \) \( \mu m \). Since the difference in \( I_d \) is more than one order of magnitude, we can assume that the \( I-V \) characteristics of \( W = 20 \) \( \mu m \) device represents center transistor. After the hot-carrier stress, both center and corner transistor degrade as shown in Fig. 3. Although the shift in \( V_{th} \) of corner transistor \( (W = 0.35 \) \( \mu m \) device) is larger than that of center transistor, its \( I-V \) characteristic is still incorporated in the center transistor because the amount of \( I_d \) is small. As shown in Fig. 4, difference in \( V_{th} \) shift, \( \Delta V_{th} \), after 50 min stress between \( W = 20 \) \( \mu m \) and \( W = 0.35 \) \( \mu m \) device, is less than 10 mV. Consider from the \( I-V \) characteristics shown in Fig. 1, more than 200 mV of \( \Delta V_{th} \) requires to observe kink in \( I-V \) for \( W = 20 \) \( \mu m \) device. If hot-carrier stress is applied more than 1000 min, kink will appear in the \( I-V \).
Fig. 5. Stress time dependence of $\Delta V_{th}$ for $W/L = 20\,\mu m/0.3\,\mu m$, $W/L = 20\,\mu m/0.35\,\mu m$, and $W/L = 0.35\,\mu m/0.3\,\mu m$ pMOSFET’s. The $W/L = 0.35\,\mu m$ device exhibits larger degradations compared to the $W/L = 20\,\mu m/0.3\,\mu m$ device though the gate length is longer.

Fig. 6. Channel width dependence of $\Delta I_{dsat}/I_{dsat}$ as a parameter of initial gate current ($I_{g0}$) which is normalized to the channel width. Narrow width device shows larger degradation for each stress condition.

Fig. 7. Channel width dependence of the normalized gate ($I_{g0}$), substrate ($I_{sub0}$), and drain ($I_{d0}$) current. Although the $I_{sub0}$ does not have channel width dependence, both $I_{g0}$ and $I_{d0}$ decrease as the device width becomes narrower.

Fig. 8. The gate current change during hot-carrier stress decreases faster for the narrow width device.

If the gate current of the narrow width device is larger than that of the wide width device, the narrow width device shows larger $I_{dsat}$ degradation. In order to investigate these enhanced degradation at narrow width region in detail, channel width dependence of each gate ($I_{g0}$), substrate ($I_{sub0}$), and drain ($I_{d0}$) current at $t = 0$ are shown in Fig. 7, where $I_{g0}$ and $I_{sub0}$ are measured at $V_d = -4.6\,V$ under $I_{gmax}$ condition and each current is normalized to the channel width. Although $I_{sub0}/W$ is uniform all over the channel width, $I_{g0}/W$ and $I_{d0}/W$ become smaller as the $W$ decreases. The values of $I_{g0}/W$ and $I_{sub0}$ for $W = 0.35\,\mu m$ device are the half of those for $W = 20\,\mu m$ device. Thus, the impact ionization rate at narrow width device is smaller than that of wide width device by channel electric filed modulation [4] and the hot-carrier density is not enhanced in the narrow width device. The same result was reported for $n$MOSFET’s [4]. However, a smaller $I_{d0}/W$ may still result in a larger $\Delta I_{dsat}/I_{dsat}$ if $I_g$ increases during the hot-carrier stress. This is the situation for nMOSFET’s where $I_{sub}$ increases during the stress in narrow width devices, while $I_{sub}$ decreases in wide width devices [4].

Fig. 8 shows the gate current change rate $I_{g}/I_{g0}$ during the stress for each channel width. The stress condition is $V_d = -4.6\,V$ at $I_{gmax}$ condition. It is evident that the $I_{g}/I_{g0}$ decreases faster in narrow width device than in wide device which is different from $\eta$MOSFET result. According
Fig. 9. Fowler–Nordheim stress results for both wide and narrow width device. Narrow device shows larger electron trapping efficiency, explained by large $\Delta V_g$.

to the $I_g$ data shown in Figs. 7 and 8, the gate oxide film of the narrow width device experiences less injected charge, $Q_{\text{inj}}(\equiv \int I_g \, dt)$, during the stress. In spite of the smaller $Q_{\text{inj}}$, narrow width device shows larger $I_{\text{sat}}$ degradation and $V_{\text{th}}$ shift (Figs. 2 and 4). However, these hot-carrier stress data cannot explain enhanced degradation in narrow region. The other considerable reason of enhanced degradation in narrow width region is the difference of the gate oxide film quality compare to the wide width device. Next, we present Fowler–Nordheim (F–N) stress results to confirm this hypothesis.

B. Fowler-Nordheim Stress Results

We hypothesize that the electron trapping efficiency of the gate oxide film is higher in the narrow width device. In order to examine the trap generation efficiency, we applied constant gate current stress $I_g/W = -50 \, \text{mA/cm}^2$ for both $W = 0.35 \, \mu\text{m}$ and $W = 20 \, \mu\text{m}$ devices. The source, drain, and substrate are tied to the ground. The shift in $V_g$ is shown in Fig. 9. As the current stress is applied, the $V_g$ is increase. Comparing the time to reach $\Delta V_g = 0.05 \, \text{V}$, $W = 0.35 \, \mu\text{m}$ device shows more than 10 times shorter time which account for higher trapping efficiency of the gate oxide film [10]. Another evidence of greater trapping efficiency is offered in Fig. 8, where $I_g$ decreases faster for the narrow channel width device though it shows large amount of degradation. The above analysis suggest that the higher efficiency of electron trapping accounts for the worse hot-carrier reliability in narrow width device with STI structure. Hamada et al. reported about the mechanical stress effect to the hot-carrier reliability [11]. However, their study focused on the gate length dependence of the hot-carrier reliability and concluded that mechanical stress dependence became small when the device size was scaled down.

Recently, Miura et al. [12] reported that the mechanical stress causes TDDDB characteristic degradation for the gate oxide film [12]. According to that paper, if the mechanical stress which applied to the MOS device exceeds certain amount of value, it causes drastic decrease of TDDDB characteristics which means large electron trapping efficiency. This mechanical stress comes from the gate electrode. However, both narrow and wide device used in our experiment have the same gate structure. More over, the narrow width device has smaller gate width which results in small mechanical stress. Consequently, mechanical stress caused by the gate electrode cannot explain enhanced hot-carrier induced degradation in narrow width device. Another considerable mechanical stress is by the trench filling materials. The residual mechanical stress by the trench filling material cause shallow defect in channel region only for small dimension device [13]. Although our device applied high temperature annealing to prevent this phenomenon, residual mechanical stress still exist in the device. We carried out the device simulation to estimate the mechanical stress caused by the trench filling material.

C. Mechanical Stress Simulation

We used process simulator Silvaco ATHENA in order to simulate shear stress at the channel surface (SiO$_2$/Si) region ($a-d'$) as shown in the Fig. 10. The trench depth of $0.7 \, \mu\text{m}$ and $T_{\text{ox}} = 6 \, \text{nm}$ were used. According to the [12], the critical shear stress which cause TDDDB characteristic degradation is around 150 MPa. Therefore, we chose the value of 150 MPa as a criteria. Fig. 10 shows the channel width dependence of the simulated shear stress. $Y$ axis indicate the percentage of the channel area which occupied by the shear stress more than 150 MPa. As clearly shown in the figure, more than 60% area is occupied by large (>150 MPa) shear stress for $W = 0.35 \, \mu\text{m}$ device while $W = 20 \, \mu\text{m}$ device is estimated less than 10%. This simulation result supports our measurement results and responsible for the enhanced hot-carrier induced degradation in narrow width region.

IV. CONCLUSIONS

Channel width dependence of the hot-carrier induced degradation in pMOSFET with STI structure has been investigated. Narrow width device shows significantly worse hot-carrier reliability compare to the wide width device even if the gate length is longer. Compare at the same gate length, the amount of $I_g$ degradation for minimum width device is more than twice that of wide width device. The impact ionization rate of the narrow width device is smaller than the wide width.
device and show lower $I_d/W$ and $J_{ach}/W$. Enhanced electron trapping efficiency of the gate oxide film in the narrow width device appears to be the cause of this phenomenon. Mechanical stress caused by STI may be responsible for this enhanced trapping efficiency and larger hot-carrier induced degradation in narrow width device.

REFERENCES


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