A Long-Refresh Dynamic/Quasi-Nonvolatile Memory Device with 2-nm Tunneling Oxide

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Abstract—A memory device using silicon rich oxide (SRO) as the charge trapping layer for dynamic or quasi-nonvolatile memory application is proposed. The device achieved write and erase speed at low voltage comparable to that of a dynamic-random-access memory (DRAM) cell with a much longer data retention time. This device has a SRO charge trapping layer on top of a very thin tunneling oxide (<2 nm). Using the traps in the SRO layer for charge storage, a symmetrical write/erase characteristics were achieved. This new SRO cell has an erase time much shorter than values of similar devices reported in the literature.

Index Terms—Nonvolatile memory device, thin oxide memory.

I. INTRODUCTION

DYNAMIC-RANDOM-ACCESS MEMORY (DRAM) is a major semiconductor product used in computer core memory. The stored charge in conventional DRAM is subject to charge loss due to carrier generation/recombination and single-event upset. The major difficulties in DRAM scaling are to maintain a large storage capacitance, which requires complicated process steps and to provide long refresh time for low-power operation [1]–[4]. The nonvolatile memory (NVM), such as flash memory, has simpler cell structure; however, its slow write and erase time limits its application [5], [6]. To ensure nonvolatility (ten-year data retention time) in NVM device, the tunneling oxide thickness has to remain above 7 nm [7] which limits the erase voltage to higher than 10 V. In some EEPROM cells, the write times can be reduced to microseconds by employing hot-electron injection. However, the erase time is limited by the low tunneling current through the relatively thick oxide and has remained in the millisecond range [8]. When the oxide thickness becomes lower than 35 Å where direct tunneling mechanism dominates, a large amount of current can pass through the thin oxide at relatively low voltage. In addition, the charge-to-breakdown increases drastically [9]. These characteristics of ultrathin oxide allow us to design devices to achieve fast write/erase speed and high endurance. Due to the relatively large direct tunneling current at low gate voltage, the expected data retention time can be shortened to minutes or seconds. Hence the concept of a long refresh dynamic memory or quasi-NVM was proposed [10]. Charge storage layers using silicon and germanium nanocrystals were fabricated by implantation [12], [13]. However, these nanocrystal memory cells have erase time in the range of ms which is not suitable for dynamic memory application. In this work, we demonstrate a quasi-NVM cell which has both fast program and erase times. This was accomplished by depositing the silicon rich oxide (SRO) layer using LPCVD [11], [13] avoiding the problem of introducing excess silicon by implantation. The memory device exhibits long refresh time and good endurance as well.

II. EXPERIMENT

The cross section of the SRO memory cell shown in Fig. 1 consists of a very thin tunneling oxide (<2.5 nm), a silicon rich oxide layer, and a high-temperature oxide (HTO) layer. Both the LPCVD SRO layer and top oxide layer are very thin (less than 10 nm) in order to achieve low write and erase voltage. The SRO films are traditionally deposited by N/O and silane gas in LPCVD process at around 650 °C [14]; however, this process results in high growth rate which is hard to control for thin film deposition (less than 10 nm). In this study, dichrosilane gas is used instead of silane for both SRO and HTO deposition at 800 °C. By changing the gas ratio, silicon dioxide can also be deposited at the same furnace step. The HTO deposited by LPCVD at this temperature shows better oxide quality, which is essential to the data retention characteristics of the memory cell.

III. RESULTS AND DISCUSSION

The ultrathin tunnel oxide conducts very high tunneling current and its charge-to-breakdown increases dramatically due to less oxide damage in the direct tunneling regime [15]. These facts point to a possibility of using floating gate device structure to achieved fast WRITE/ERASE speed for dynamic memory application [10]. Applying the measured tunneling current characteristics and charge-to-breakdown characteristics
Performance of a single floating gate cell are estimated by using the tunneling current and charge-to-breakdown characteristics for the thin oxides. The WRITE/ERASE voltage is assumed to be 5 V with control oxide equals to 50 Å. The data retention time is calculated by assuming zero gate voltage.

Fig. 2.

Uncharged threshold voltage of this cell is designed to be 0.4 V. With a 100 ns, 6-V voltage pulse, the threshold voltage shift can reach as high as 1 V.

Fig. 3. The WRITE/ERASE speed, data retention time and endurance (oxide breakdown as the cycle limit) were estimated. Fig. 2 shows that by simple reducing the tunneling oxide in the floating gate structure to gain W/E speed, the device will lose its benefit of a longer refresh time than that of a DRAM cell. The charge traps formed by silicon islands in the silicon rich oxide is therefore chosen instead of a poly-silicon floating gate as the data storage medium in an effort to achieved longer refresh.

Fig. 4. The WRITE/ERASE time achieved by the cell under various operation voltage. For WRITE/ERASE voltage at 5 V, the WRITE/ERASE speed reaches 100 ns with 0.5 threshold voltage shift.

IV. CONCLUSION

A new SRO dynamic memory cell with fast WRITE/ERASE speed and long refresh time is proposed and fabricated. Using a thin tunneling oxide and charge trapping film, at 5 V WRITE/ERASE voltage, less than 100 ns WRITE/ERASE time can be achieved. We have shown that the SRO memory device is a promising candidate for low-power DRAM replacement or as a quasi-nonvolatile cell when a thicker tunneling oxide is chosen.

REFERENCES