0.35-μm Asymmetric and Symmetric LDD Device Comparison Using a Reliability/Speed/Power Methodology

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Abstract—The reliability and performance of NMOSFET asymmetric LDD devices (with no LDD on the source side) are compared with that of conventional LDD devices. The results show that asymmetric LDD devices exhibit higher \( I_{\text{d sat}} \) and larger \( I_{\text{subh}} \). To maintain the same hot-carrier lifetime, asymmetric LDD devices must operate at lower \( V_{\text{dd}} \). For the same hot-carrier lifetime, we show that ring oscillators with asymmetric LDD devices can achieve 5% (10% if PMOSFET also had asymmetric LDD) higher speed and 10% lower power.

Index Terms—Hot carriers, integrated circuit reliability, semiconductor device reliability.

I. INTRODUCTION

LDD structures [1] in MOSFET are commonly used to improve hot-carrier reliability of submicron devices. However, the transistor current is reduced due to the parasitic resistance in the LDD region. The device characteristics and reliability of asymmetric LDD (lightly doped region on the drain side only) devices has been studied in the past for 0.5-μm technology [2], [3]. As MOS devices are scaled to deep submicron regime, this parasitic resistance may impose a greater detrimental effect to the driving current. Also because of the recent industry emphasis on high speed product/technology, it is critically important to optimize the LDD design for maximum current-drive capability, while maintaining acceptable hot-carrier reliability [4]–[6]. We decided to reexamine the asymmetric LDD study with a 0.35-μm technology and compare it with conventional LDD devices in a reliability-speed-power comparison that is appropriate for today’s device optimization methodology.

In this work, individual devices and ring oscillators with asymmetric and conventional LDD structures were fabricated. Accelerated DC stressing were performed on individual devices to evaluate the device reliability. The delay and power of ring oscillators were measured under various supply voltages \( (V_{\text{dd}}) \). Finally, the delay and power were compared under the constraint of equal hot-carrier lifetime to quantify the benefit of using asymmetric LDD devices.

Fig. 1. The \( I_d-V_d \) and \( I_{\text{subh}}-V_{\text{gs}} \) characteristics show that asymmetric LDD devices exhibit greater \( I_{\text{d sat}} \) and also \( I_{\text{subh}} \), indicating higher driving capability but shorter hot-carrier lifetime.

II. EXPERIMENTS

Individual devices and ring oscillators with asymmetric and conventional LDD structures were fabricated by an advanced 0.35-μm dual-poly gate CMOS process with 0.3-μm gate length and 60 Å gate oxide thickness. Test structures with asymmetric LDD devices were implemented for NMOS devices. The process requires the alignment of a photoresist implant mask to the transistor gate with a precision better than the gate length. This is well within the capability of lithography tools. PMOS devices have the conventional LDD design. Several individual NMOS devices were stressed for hot-carrier reliability characterization. The saturation drain current \( (I_{\text{d sat}}) \) was measured at \( V_{\text{gs}} = V_{\text{dd}} = 2.7 \) V and used as the degradation monitor. Hot-carrier lifetime was defined to be the time to reach 10% degradation in \( I_{\text{d sat}} \). The lifetimes obtained under stress voltages were then used to extrapolate the lifetimes under other voltages. The inverter ring oscillators with one fan-out and \( W_n/W_p = 5 \) μm/10 μm consist of 101 stages. The delay and power of several ring oscillators were measured and the average values are reported here for each \( V_{\text{dd}} \).

III. RESULTS AND DISCUSSION

The \( I_d-V_d \) and \( I_{\text{subh}}-V_{\text{gs}} \) characteristics of an asymmetric and a conventional LDD NMOS devices are shown in Fig. 1, where \( I_d \) was measured at \( V_{\text{gs}} = 2.7 \) V, while \( I_{\text{subh}} \) was

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The degradation rates of asymmetric and conventional LDD devices are identical, with roughly 2.5 times shorter in hot-carrier lifetime for the asymmetric LDD devices.

The hot-carrier lifetime of both asymmetric and conventional LDD devices can be described by \( \tau \propto (I_{sat}/W)^{-2.8} \).

measured at \( V_{ds} = 3.75 \, V \). 12\% increase in \( I_{sat} \) was observed for the asymmetric LDD device. This compares with 36\% for a 0.45 \( \mu \)m device [6]. On the other hand, the asymmetric LDD device also introduces 30\% higher \( I_{sub} \), indicating shorter hot-carrier lifetime at a fixed \( V_{ddl} \). Fig. 2 shows the forward-mode \( I_{sat} \) degradation of both types of devices under stressing at \( V_{ds} = 3.75 \, V \). The two slopes are equal, with roughly 2.5 times shorter in lifetime for the asymmetric LDD device. The lifetime versus \( I_{sub}/W \) plot was drawn in Fig. 3. From the figure, the identical \( \tau-I_{sub} \) relationship is followed by both types of devices. The results shown in Figs. 2 and 3 suggest that no new degradation mechanism is introduced for asymmetric LDD structures. \( I_{sub} \) can be used as a lifetime predictor for different LDD designs provided the design of LDD region is identical on the drain side.

Since devices with asymmetric LDD structures show higher \( I_{sat} \) but shorter lifetime, a fair comparison between the two types of devices should be made under the constraint of equal hot-carrier lifetime. Fig. 4 shows the lifetime as a function of \( I_{sat} \) with \( V_{ddl} \) as the variable, where \( V_{ddl} = 2.7, 3, \) and 3.3 \( V \). The results show that to maintain the same lifetime such as ten years as drawn in Fig. 4, 0.12 \( V \) lower \( V_{ddl} \) must be applied to asymmetric LDD devices, but 8\% greater \( I_{sat} \) is still retained even at the lower \( V_{ddl} \). This suggests that the speed of ring oscillators may be faster for asymmetric LDD devices because \( V_{ddl} \) is lower and \( I_{sat} \) is greater and for an inverter,

\[
t_{pHIL} \propto \frac{CV_{ddl}}{I_{sat},n}
\]

where \( t_{pHIL} \) is the response time for high-to-low output transition, and \( C \) is the load capacitance. This argument is confirmed in Fig. 5, where the delay (\( t_p \)) and power per MHz (\( P \)) of the ring oscillators under \( V_{ddl} = 2.7, 3, \) and 3.3 \( V \) were drawn. The results show that for the same hot-carrier lifetime, roughly 5\% faster in speed and 10\% lower in power can be obtained for the ring oscillators with asymmetric LDD devices. Since no asymmetric LDD PMOS devices were fabricated, the difference in \( t_p \) is due to the difference in \( t_{pHIL} \). Using (1) with 5\% decrease in \( t_p \), 8\% increase in \( V_{ddl} \), 5\% decrease in \( V_{ddl} \), and assume \( \Delta t_p/t_p = (\Delta t_{pHIL}/t_{pHIL})/2 \), we deduce that \( C \) is identical for both asymmetric and conventional LDD devices. This is reasonable because the source-gate overlap capacitance increased by the same amount that the
channel-gate capacitance decreased. Note the above analysis of $\Delta t_p/t_p [1 - (1 - 0.05)/(1 + 0.08)]/2 \approx 6\%$, is 1% higher than the experimental data, which may be the result of approximation involved in (1). Since $P \propto CV_{th}^2$ and $V_{th}$ decreased by 5% and $C$ remained the same, we expect $P$ to decrease by 10%—in exact agreement with measurement. The above results indicate that using asymmetric LDD devices can improve circuit speed and power consumption without sacrificing reliability and is thus an interesting alternative in implementing high performance technology.

IV. Conclusions

The reliability and performance of asymmetric LDD devices were investigated. Asymmetric LDD devices exhibit higher $I_{kat}$ and also larger $I_{sub}$. Under the same $I_{sub}$ conditions, asymmetric and conventional LDD devices exhibit the same lifetime. For devices with the same hot-carrier lifetime and channel length, circuits with asymmetric LDD structures can operate at lower $V_{th}$, 10% lower power, and 5% higher speed (10% higher speed if PMOS also has asymmetric LDD).

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