A Physical and Scalable $I$–$V$ Model in BSIM3v3 for Analog/Digital Circuit Simulation

Yuhua Cheng, Member, IEEE, Min-Chie Jeng, Member, IEEE, Zihong Liu, Member, IEEE, Jianhui Huang, Mansun Chan, Kai Chen, Member, IEEE, Ping Keung Ko, Fellow, IEEE, and Chenming Hu, Fellow, IEEE

Abstract—A new physical and continuous BSIM (Berkeley Short-Channel IGFET Model) $I$–$V$ model in BSIM3v3 is presented for circuit simulation. Including the major physical effects in state-of-the-art MOS devices, the model describes current characteristics from subthreshold to strong inversion as well as from the linear to the saturation operating regions with a single $I$–$V$ expression, and guarantees the continuities of $I_{ds}$, conductances and their derivatives throughout all $V_{gs}$, $V_{ds}$, and $V_{th}$ bias conditions. Compared with the previous BSIM models, the improved model continuity enhances the convergence property of the circuit simulators. Furthermore, the model accuracy has also been enhanced by including the dependencies of geometry and bias of parasitic series resistances, narrow width, bulk charge, and DIBL effects. The new model has the extensive built-in dependencies of important dimensional and processing parameters (e.g., channel length, width, gate oxide thickness, junction depth, substrate doping concentration, etc.). It allows users to accurately describe the MOSFET characteristics over a wide range of channel lengths and widths for various technologies, and is attractive for statistical modeling. The model has been implemented in the circuit simulators such as Spectre, Hspice, SmartSpice, Spice3e2, and so on.

I. INTRODUCTION

As the development of MOS VLSI technology progresses, the circuit designers need models for advanced MOSFET’s for use in circuit simulators such as SPICE. The continuity, accuracy, scalability, and simulation performance are basic requirements for a MOSFET model to meet the needs of analog and mixed analog/digital circuit designs [1], [2].

Some models, including several previous versions of BSIM that have been developed and implemented in SPICE for use in circuit simulation [3]–[5], use separate model expressions for such device operation regimes as subthreshold and strong inversion. The expressions can accurately describe device behavior within their own respective region of operation. However, problems can occur in transition regions between well-described subthreshold and strong inversion regions. In order to circumvent this issue, a new BSIM model should be synthesized to not only preserve region-specific device physics but also to ensure the continuities of current ($I_{ds}$) and conductance ($G_{ds}$) and their derivatives in all terminal voltages to prevent nonphysical results in circuit simulation.

Several continuous MOSFET models have been reported [6]–[8]. In this paper, we present the $I$–$V$ model in BSIM3v3 for use in the analog/digital circuit simulation. Retaining the advanced features of the previous BSIM model, this new model describes current characteristics from subthreshold to strong inversion as well as from the linear to the saturation operating regions with a single expression, and guarantees the continuities of $I_{ds}$ conductances and their derivatives throughout all $V_{gs}$, $V_{ds}$, and $V_{th}$ bias conditions. Furthermore, the model accounts for all the major physical effects in state-of-the-art MOSFET devices such as threshold voltage roll-off, nonuniform doping effect, mobility reduction due to vertical field, carrier velocity saturation, CLM, DIBL, SCBE, subthreshold conduction, parasitic resistance effect, and so on. The new model has extensive built-in dependencies of important dimensional and processing parameters (e.g., channel length, width, gate oxide thickness, junction depth, substrate doping concentration, etc.) This allows users to accurately model the MOSFET over a wide range of channel lengths and widths for various technologies, and is suitable for the statistical modeling use.

II. MODEL

A. Continuous Channel Charge Density Expression

Separate expressions for channel charge density in strong inversion and subthreshold regions at small $V_{ds}$ were used in previous BSIM models as follows [3]–[5]:

\[
\begin{align*}
Q_{ch0} &= C_{ox} (V_{gs} - V_{th})^2, & V_{gs} > V_{th} \\
Q_{ch0} &= \sqrt{\frac{e}{2}\frac{N_{ch}}{m^*}} \exp \left( \frac{V_{gs} - V_{th} - V_{off}}{n^*} \right), & V_{gs} < V_{th}\end{align*}
\]

(1)

(2)

Here, the parameter $n^*$ is the thermal voltage and is given by $kT/q$, $N_{ch}$ is the channel doping concentration, $\Psi_s$ is called as twice the Fermi potential and is given by $2\mu q \ln(N_{ch}/n_i)$: $V_{off}$ represent the small difference between the “threshold voltages” in the strong inversion and the subthreshold regimes [4], $n_i$ is the subthreshold swing parameter, which is a function of body bias, channel length and the interface state density, $V_{th}$.
is the threshold voltage of the device and is given as follows [9], [10]:

\[ V_{th} = V_{thc} + K_1 \left( \sqrt{\Psi_s - V_{bs}} - \sqrt{\Psi_s} \right) - K_2 V_{bs} + K_1 \left( \sqrt{1 + \frac{N_{ox}}{L_{eff}}} - 1 \right) \sqrt{\Psi_s} + (K_3 + K_{3b} V_{bs}) \frac{T_{ox}}{W_{eff} + W_0} \Psi_s - D_{VT0} \left[ \exp \left( -D_{VT1} \frac{L_{eff}}{2L_t} \right) + 2 \exp \left( -D_{VT1} \frac{L_{eff}}{L_t} \right) \right] (V_{bt} - \Psi_s) - D_{VT0} \left[ \exp \left( -D_{VT1} \frac{L_{eff}}{L_t} \right) + 2 \exp \left( -D_{VT1} \frac{L_{eff}}{2L_t} \right) \right] (V_{bs} - \Psi_s) - \left[ \exp \left( -D_{sub} \frac{L_{eff}}{2L_t} \right) + 2 \exp \left( -D_{sub} \frac{L_{eff}}{L_t} \right) \right] \cdot (E_{tao} + E_{tab} V_{bs}) V_{ds} \]  
(3)

where \( V_{thc} \) is the threshold voltage for a long-channel device, \( T_{oxc} \) is the thickness of gate oxide, \( V_{gs} \) is the built-in potential of drain/source-body junction, \( L_t \) and \( L_{to} \) are functions of \( T_{oxc} \), channel doping concentration and body bias. \( K_1, K_2, D_{VT0}, D_{VT1}, D_{VT0b}, D_{VT1b}, D_{sub}, E_{tao}, E_{tab}, W_0, K_3, K_{3b}, \) and \( N_{ox} \) are parameters to be extracted from the measured data.

Based on (1) and (2), a function named \( V_{gsteff} \) is introduced to obtain a continuous channel charge characteristics from subthreshold to strong inversion [11]

\[ V_{gsteff} = \frac{2n \Phi_n \ln \left( 1 + \exp \left( \frac{V_{gs} - V_{th}}{2n \Phi_n} \right) \right)}{1 + 2nC_{ox} \sqrt{\frac{2 \psi_s}{q \varepsilon_{si} N_{ch}}} \exp \left( -\frac{V_{gs} - V_{th} - 2V_{off}}{2n \Phi_n} \right)} \]  
(4)

\[ Q_{ch0} = C_{ox} V_{gsteff}, \quad \text{for all} \ V_{gs}. \]  
(5)

Fig. 1 shows the comparison result between measured data and the continuous charge expression (5) as well as the charge expressions of (1) and (2) in subthreshold and strong inversion regions. It can be found that (5) can describe the measured channel charge data well and match (1) and (2) in subthreshold and strong inversion regions, respectively, and has a smooth transition at the boundary of the two regions.

To account for the influence of \( V_{ds} \), consider first the usual modification of charge density in the channel for the case of strong inversion

\[ Q_{ch0}(y) = C_{ox} \left[ V_{gs} - V_{th} - A_{bulk} V_{F(y)} \right], \]  
(6)

The parameter \( V_{F(y)} \) stands for the quasi-Fermi potential at any given point, \( y \), along the channel with respect to the source. \( A_{bulk} \) accounts for the bulk charge effect and is given by

\[ A_{bulk} = \left( 1 + \frac{K_1}{2 \sqrt{\Psi_s - V_{bs}}} \left\{ \frac{A_0 L_{eff}}{L_{eff} + 2 \sqrt{X_J X_{dep}}} \right\} \cdot \left( 1 - A_{gs} V_{gsteff} \left( \frac{L_{eff} + 2 \sqrt{X_J X_{dep}}} {L_{eff} + 2 \sqrt{X_J X_{dep}}} \right)^2 \right) \right) \frac{1}{1 + K_{ETA} V_{bs}}, \]  
(7)

where \( A_0, A_{gs}, B_0, B_1, \) and \( K_{ETA} \) are to be extracted from measured \( I-V \) data.

For the subthreshold region \( (V_{gs} \ll V_{th}) \), the channel charge density along the channel from source to drain can be written as

\[ Q_{ch0}(y) = \sqrt{\frac{q \varepsilon_{si} N_{ch}}{2 \psi_s}} \nu_t \exp \left[ \frac{V_{gs} - V_{th} - A_{bulk} V_{F(y)}}{n \Phi_n} \right]. \]  
(8)

With a Taylor series expansion of the exponential term at very small \( V_{ds} \ (V_{ds} < 2 \Phi_n) \), (8) yields the following (keeping only the first two terms):

\[ Q_{ch0}(y) = \sqrt{\frac{q \varepsilon_{si} N_{ch}}{2 \psi_s}} \nu_t \exp \left( 1 - \frac{A_{bulk} V_{F(y)}}{n \Phi_n} \right). \]  
(9)

Note that (9) is valid when \( V_{F(y)} \) is very small. Fortunately, (9) is adequate due to the fact that (9) is only used in the so called linear regime (i.e., \( V_{ds} \leq 2 \Phi_n \) in the subthreshold regime. [For \( V_{ds} \gg \Phi_n \), the subthreshold current is independent of \( V_{ds} \) except for the drain-induced barrier lowering effect modeled by (3)].
Based on (1), (2), (4)–(6), and (9), a continuous expression for $Q_{ch(y)}$ from subthreshold to strong inversion regimes can be obtained

$$Q_{ch(y)} = Q_{ch0} \left[ 1 - \frac{V_{F(y)}}{V_b} \right]$$  \hspace{1cm} \text{(10)}

where $V_b = (V_{gsteff} + n^2 V_b)/A_{bulk}$. Generally, $n$ is 1–2 and has a drain and body bias dependencies. In order to improve the calculation efficiency of the model, we replace the variable $n$ with 2 in $V_b$, and the expression for $V_b$ now becomes

$$V_b = \frac{V_{gsteff} + 2V_b}{A_{bulk}}.$$  \hspace{1cm} \text{(11)}

### B. Continuous Mobility Expression

Based on the mobility model in the strong inversion regime [5], a continuous mobility model with the above $V_{gsteff}$ expression is shown as follows:

$$\mu_{eff} = \frac{\mu_o}{1 + U_d \left( \frac{V_{gsteff} + 2V_b}{T_{ox}} \right) + U_b \left( \frac{V_{gsteff} + V_b}{T_{ox}} \right)^2 + U_c V_b s}$$  \hspace{1cm} \text{(12)}

where $\mu_o$, $U_d$, $U_b$, and $U_c$ are extracted parameters. $T_{ox}$ is the thickness of gate oxide. This mobility expression becomes a constant value in the subthreshold region, and ensures no mobility discontinuity.

### C. Effective Channel Length and Width

The effective channel length and width used in the model is

$$L_{eff} = L_{drawn} - 2dL$$  \hspace{1cm} \text{(13)}

$$W_{eff} = W_{drawn} - 2dW$$  \hspace{1cm} \text{(14)}

where $dW$ and $dL$ are further modeled with the following expressions to improve the model accuracy in wide $W$ and $L$ ranges:

$$dL = L_{int} + \frac{L_d}{L_{int}} + \frac{L_w}{W_{L_{drawn}}} + \frac{L_{dd}}{L_{int} W_{L_{drawn}}}$$  \hspace{1cm} \text{(15a)}

$$dW = W_{int} + dW_g V_{gsteff}$$

$$+ dW_b \left( \sqrt{\Psi_S - V_{bs}} - \sqrt{\Psi_S} \right)$$

$$+ \frac{W_l}{L_{w}} + \frac{W_s}{W_{L_{drawn}}}$$

$$+ \frac{W_{ul}}{L_{w} W_{L_{drawn}}}$$  \hspace{1cm} \text{(15b)}

where $W_{int}$, $dW_g$, $dW_b$, $W_l$, $W_w$, $W_{L_{drawn}}$, $W_{ul}$, $L_{int}$, $L_d$, $L_w$, $L_{L_{drawn}}$, and $L_{ul}$ are extractable parameters. One may choose to use a simplified form of $dW$ without the bias dependencies by setting $dW_g$ and $dW_b$ to be zero

$$dW' = W_{int} + \frac{W_l}{L_{w}} + \frac{W_w}{W_{L_{drawn}}} + \frac{W_{ul}}{L_{w} W_{L_{drawn}}}.$$  \hspace{1cm} \text{(16b)}

### D. Continuous Linear Current Expression

1) Intrinsic Case ($R_{ds} = 0$): Generally, the following expression is used to account for both drift and diffusion current in the linear region:

$$I_{d(y)} = W Q_{ch(y)} \mu_{ne(y)} \frac{dV_{F(y)}}{dy}$$  \hspace{1cm} \text{(17)}

where the parameter $\mu_{ne(y)}$ can be considered as the effective mobility including the influence of the lateral electrical field $E_y$ along the channel, and can be written as

$$\mu_{ne(y)} = \frac{\mu_{eff} \mu_{o}}{1 + \frac{E_y}{E_{sat}}}$$  \hspace{1cm} \text{(18)}

where $E_{sat} = 2V_{sat}/\mu_o$ and corresponds to the critical electrical field at which the carrier velocity becomes saturated. $V_{sat}$ is the carrier saturation velocity.

Substituting (18) in (17), we get

$$I_{d(y)} = W_{eff} \mu_{eff} Q_{ch0} V_b \left[ 1 - \frac{V_{F(y)}}{V_b} \right] \frac{\mu_{eff}}{1 + \frac{E_y}{E_{sat}}} \frac{dV_{F(y)}}{dy}.$$  \hspace{1cm} \text{(19)}

Equation (19) can be integrated from the source to drain to get the expression for linear drain current in the channel. This expression is valid from the subthreshold regime to the strong inversion regime

$$I_{ds0} = \frac{W_{eff} \mu_{eff} Q_{ch0} V_b \left( 1 - \frac{V_{ds}}{2V_b} \right)}{L_{eff} \left( 1 + \frac{V_{ds}}{E_{sat} L_{eff}} \right)}.$$  \hspace{1cm} \text{(20)}

2) Extrinsic Case ($R_{ds} > 0$): The devices with series resistances make the modeling more difficult. A straightforward and accurate way of modeling parasitic resistance effect will lead to a complicated drain current expression. In order to make model equation simpler, BSIM3 models the parasitic resistance using a simple way with some approximation. The continuous intrinsic current expression (20) for linear drain current from subthreshold to strong inversion can be modified for the influence of the parasitic series resistance $R_{ds}$ [5]

$$I_{ds} = \frac{I_{ds0}}{1 + \frac{R_{ds} I_{ds0}}{V_{ds}}}$$  \hspace{1cm} \text{(21)}

where the parasitic resistance $R_{ds}$ is modeled as

$$R_{ds} = \frac{R_{ds0} [1 + P_{r wg} V_{gsteff} + P_{r ub} (\sqrt{\Psi_s - V_{bs}} - \sqrt{\Psi_s})]}{W_{eff}}$$  \hspace{1cm} \text{(22)}

where $R_{ds0}$ is the resistance per unit width and can be extracted from the measured data together with the parameters $W_r$, $P_{r wg}$, and $P_{r ub}$. 
E. Continuous Saturation Voltage ($V_{\text{dsat}}$) Expression

1) Intrinsic Case ($R_{ds} = 0$): To get an expression for the electric field as a function of the position $y$ along the channel, we integrate (19) from 0 to an arbitrary point $y$. The expression is as shown in (23) at the bottom of the page. If we assume that the drift velocity saturates when $E_y = E_{\text{sat}}$, we get the following expression for $I_{\text{dsat}}$ from (23):

$$I_{\text{dsat}} = \frac{W_{\text{eff}} Q_{\text{ch10}} E_{\text{sat}} V_{b}}{2(E_{\text{sat}} L_{\text{eff}} + V_{b})}. \quad (24)$$

Let $V_{ds} = V_{\text{dsat}}$ in (20) and set it equal to (24), we get the following expression for $V_{\text{dsat}}$:

$$V_{\text{dsat}} = \frac{E_{\text{sat}} L_{\text{eff}} (V_{\text{gsteff}} + 2\vartheta)}{A_{\text{bulk}} E_{\text{sat}} L_{\text{eff}} + V_{\text{gsteff}} + 2\vartheta}. \quad (25)$$

2) Extrinsic Case ($R_{ds} > 0$): Following the steps leading to (25), with the influence of the parasitic series resistance $R_{ds}$, the $V_{\text{dsat}}$ expression for the extrinsic case is

$$V_{\text{dsat}} = \frac{E_{\text{sat}} L_{\text{eff}} (V_{\text{gsteff}} + 2\vartheta)}{A_{\text{bulk}} E_{\text{sat}} L_{\text{eff}} + V_{\text{gsteff}} + 2\vartheta}. \quad (26)$$

where

$$a = A_{\text{bulk}}^2 W_{\text{eff}} E_{\text{sat}} C_{\text{ox}} R_{DS} + \left(\frac{1}{\lambda} - 1\right) A_{\text{bulk}} \quad (27)$$

$$b = -\left[(V_{\text{gsteff}} + 2\vartheta) \left(\frac{2}{\lambda} - 1\right) + A_{\text{bulk}} E_{\text{sat}} L_{\text{eff}} + 3A_{\text{bulk}} (V_{\text{gsteff}} + 2\vartheta) W_{\text{eff}} E_{\text{sat}} C_{\text{ox}} R_{DS}\right] \quad (28)$$

$$c = \left(V_{\text{gsteff}} + 2\vartheta\right) E_{\text{sat}} L_{\text{eff}} + 2(V_{\text{gsteff}} + 2\vartheta)^2 W_{\text{eff}} E_{\text{sat}} C_{\text{ox}} R_{DS} \quad (29)$$

$$\lambda = A_1 V_{\text{gsteff}} + A_2 \quad (30)$$

The parameter $\lambda$ is introduced to account for nonsaturation effects in the devices. The parameters $A_1$ and $A_2$ are extracted from the measured data.

F. Continuous Saturation Current Expression

As discussed in [5], [10], there are three physical mechanisms which affect the output resistance in the saturation region: channel length modulation (CLM), drain-induced barrier lowering (DIBL), and the substrate current induced body effect (SCBE). We can use the following equation to describe the current in the saturation region ($V_{ds} > V_{\text{dsat}}$) [5], [10]:

$$I_{\text{ds}}(V_{gs}, V_{ds}) = I_{\text{dsat}} \left(1 + \frac{V_{ds} - V_{\text{dsat}}}{V_A}\right) \quad (31)$$

where the parameter $V_A = I_{\text{dsat}} (\partial I_{\text{dsat}}/\partial V_{ds})^{-1}$.

If channel length modulation is the only physical mechanism to be taken into account, the $V_A$ (written as $V_{\text{A\text{CLM}}}$) can be given as the following based on a quasi-two-dimensional model [5], [10]:

$$V_{\text{A\text{CLM}}} = \frac{A_{\text{bulk}} E_{\text{sat}} L_{\text{eff}} + V_{\text{gsteff}}}{P_{\text{CLM}} A_{\text{bulk}} E_{\text{sat}} V_{b}} (V_{ds} - V_{\text{dsat}}) \quad (32)$$

where $b = \frac{\sqrt{\varepsilon_{s0}}}{\varepsilon_{s0}} f_{\text{ox}} f_{\text{eff}}$, and $P_{\text{CLM}}$ is extracted from measured data.

DIBL is the reduction of $V_{th}$ due to a lowering of the potential barrier for carriers at the source side of the channel when $V_{gs} \leq V_{th}$. However, when $V_{gs} \geq V_{th}$, there is still a reduction of the $V_{th}$ due to the electrostatic coupling between the drain and the channel as if the drain is serving as an unwanted extra gate, that is similar to the DIBL effect accounted for in $V_{th}$. Because of this, we do not eliminate the influence of DIBL in $V_{th}$ when $V_{gs} \geq V_{th}$. In addition, we introduce a correction term in $V_A$ to further improve the accuracy of $V_{th}$ reduction in saturation region. If the reduction of $V_{th}$ in saturation is the only physical mechanism to be taken into account, the $V_A$ (written as $V_{\text{A\text{DIBL}}}$) can be given the following to meet the goal of unification of the expression in both subthreshold and strong inversion:

$$V_{\text{A\text{DIBL}}} = \frac{V_{\text{gsteff}} + 2\vartheta}{\theta_{\text{route}} \left(1 + P_{\text{DIBL,2}} V_{bs}\right)} \cdot \left(1 - \frac{A_{\text{bulk}} V_{\text{dsat}} + V_{\text{gsteff}} + 2\vartheta}{A_{\text{bulk}} V_{\text{dsat}} + V_{\text{gsteff}} + 2\vartheta}\right). \quad (33)$$

The expression for $\theta_{\text{route}}$ is

$$\theta_{\text{route}} = P_{\text{DIBL,2}} \left[\exp\left(-D_{\text{DIBL,2}} L_{\text{eff}}/2L_0\right) + 2 \exp\left(-D_{\text{DIBL,2}} L_{\text{eff}}/L_0\right)\right] + P_{\text{DIBL,2}}. \quad (34)$$

The variables $P_{\text{DIBL,1}}, P_{\text{DIBL,2}}, P_{\text{DIBL,3}}$, and $D_{\text{DIBL,2}}$ in (33) and (34) are extracted parameters.

Based on the above, the total $V_A$, due to the CLM and DIBL effects, can be written as

$$V_A = V_{\text{A\text{sat}}} + \left[1 + \frac{P_{\text{Vag}} V_{\text{gsteff}}}{E_{\text{sat}} L_{\text{eff}}} \right] \frac{1}{\left(V_{\text{A\text{CLM}}} + 1/\left(V_{\text{A\text{DIBL}}}\right)^{-1}\right)} \quad (35)$$

where $P_{\text{Vag}}$ is introduced in (35) to improve the fit of the gate bias dependence of $V_A$ with measured data. $V_{\text{A\text{sat}}}$ is the $V_A$ at $V_{ds} = V_{\text{dsat}}$, as shown in (36) at the bottom of the next page.

In the above derivation, we did not consider the substrate current ($I_{\text{sub}}$) induced body effect. $I_{\text{sub}}$ creates a forward body bias through the ohmic drop in the body. The body bias causes a $V_{th}$ drop and hence a current increase. According to $I_{\text{sub}}$
model [12], the $V_A$ due to the substrate current induced body effect can be obtained easily

$$\frac{1}{V_{ASCBE}} = \frac{P_{sc1e1}}{L_{eff}} \exp \left( -\frac{P_{sc1e2} l_i t}{V_{ds} - V_{dsat}} \right)$$ (37)

where $P_{sc1e1}$ and $P_{sc1e2}$ are similar to the $A_2$ and $B_i$ parameters given in [12], and can be extracted experimentally.

Thus, a continuous expression for the total saturation drain current, including the influence of CLM, DIBL, and SCBE, from the subthreshold to the strong inversion regime can be written as

$$I_{ds} = \frac{I_{ds}(V_{dsat})}{1 + \frac{V_{ds}}{V_{dsat}}} \cdot \left( 1 + \frac{V_{ds} - V_{dsat}}{V_{A}} \right) \left( 1 + \frac{V_{ds} - V_{dsat}}{V_{ASCBE}} \right)$$ (38)

G. Single Current Expression for All Operational Regimes of $V_{gs}$ and $V_{ds}$

In the above, we have given continuous expressions for the linear drain current and the saturation drain current from subthreshold to strong inversion, separately. Further, we want to use a single expression to describe the $I$-$V$ characteristics in whole operation regimes of $V_{gs}$ and $V_{ds}$. Continuous functions have been suggested in the past [13], [14] to describe the device characteristics from linear to saturation regime in strong inversion. In this paper, we use the following simpler $V_{dseff}$ function to link the linear current expression with the saturation current expression presented above:

$$V_{dseff} = V_{dsat} - \frac{1}{2} \left( V_{dsat} - V_{ds} - \delta \right) + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}}$$ (39)

where the parameter $\delta$ is a constant with the typical value of 0.01 V. $\delta$ is roughly 1% of the transition range between the two branches of $V_{dseff}$ as shown in Fig. 2. $V_{dseff}$ is equal to $V_{ds}$ in the linear region and become $V_{dsat}$ in the saturation region.

The overall current equation for both linear and saturation current finally can be described by the following single equation:

$$I_{ds} = \frac{I_{dio}}{1 + \frac{V_{dseff}}{V_{dsat}}} \cdot \left[ 1 + \frac{V_{ds} - V_{dseff}}{V_{A}} \right] \left( 1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}} \right)$$ (40)

where $I_{dio}$ and $V_{A}$ are given by (20) and (35), respectively, but the $V_{ds}$ terms in $I_{dio}$ and $V_{dsat}$ terms in $V_{A}$ are substituted with $V_{dseff}$.

Fig. 2. $V_{dsat}$ versus $V_{ds}$ curves at different $\delta$ values.

Fig. 3. Measured and modeled $V_{dsat}$-$V_{ds}$ characteristics of the device with $W_{drawn}/L_{drawn} = 20/0.4$ at different gate voltages.

$V_{dseff}$. The $V_{ds}$ in the threshold voltage expression and the $V_{dsat}$ in the $V_{ADIBL}$ expression are not replaced with $V_{dseff}$.

$$V_{A_{sat}} = \frac{E_{sat} L_{eff} + V_{dsat} + 2R_{DS} V_{sat} C_{ox} W_{eff} V_{gseff} \left[ 1 - \frac{A_{bulk} V_{dsat}}{2(V_{gseff} + 2\eta)} \right]}{\frac{2}{\lambda} - 1 + R_{DS} V_{sat} C_{ox} W_{eff} A_{bulk}}$$ (36)
Fig. 4. Measured and modeled $G_{ds}$–$V_{ds}$ characteristics of the device with $W_{drawn}/L_{drawn} = 20/0.4$ at different gate voltages.

Fig. 5. Measured and modeled $R_{on}/W_{ds}$ characteristics of the device with $W_{drawn}/L_{drawn} = 20/0.4$ at different gate voltages.

III. PARAMETER EXTRACTION

Parameter extraction is an important consideration for model development. Many different extraction methods have been developed [15], [16]. The appropriate methodology depends on the model and on the way the model is used. There are two main, different optimization strategies: global optimization and local optimization. Global optimization relies on the explicit use of a computer optimization algorithm to find one set of model parameters which will best fit the available measured data. In local optimization, many parameters are extracted independently of one another. Parameters are extracted at device bias conditions which highlight the value of one or a few local parameters.

Furthermore, two different strategies are available for extracting parameters: the single device extraction strategy and group device extraction strategy. In single device extraction
strategy, experimental data from a single device is used to extract a complete set of model parameters. This strategy will fit one device very well but may not fit other devices with different channel length or width. Single device strategy is often used in conjunction with “binning,” i.e., a composite model made of multiple set of model parameters, each severing a specific range of $W$ and $L$ by interpolation with different $W$ & $L$. Also, single device extraction strategy can not guarantee that the extracted parameters are the best physical fits. Group device extraction strategy would find one set of parameters that fit all $W$ & $L$.

Based on the properties of the present model, a combination of a local optimization and the group device extraction strategy is adopted for parameter extraction. This requires measured data from devices with different geometry. One large size device and three smaller devices are needed to extract parameters. One set of devices with a fixed large channel width and different channel lengths are used to extract parameters which are related to the short-channel effects. Similarly, one set of devices with a fixed long-channel length but different channel widths are used to extract parameters which are related to narrow width effects.
Regardless of device geometry, each device will have to be measured under four distinct bias conditions.

1) $I_{ds}$ versus $V_{gs} @ V_{ds} = 0.05$ V with different $V_{ds}$.
2) $I_{ds}$ versus $V_{ds} @ V_{gs} = 0$ V with different $V_{gs}$.
3) $I_{ds}$ versus $V_{gs} @ V_{ds} = V_{dd}$ with different $V_{ds}$. ($V_{dd}$ is the maximum drain voltage).
4) $I_{ds}$ versus $V_{ds}$ with different $V_{gs}$. ($V_{th}$ is the maximum body bias).

The optimization process recommended for BSIM3v3 is a combination of Newton–Raphson’s iteration and linear-squares fit of either one, two, or three variables [17].

IV. MODEL TEST RESULTS

A set of Benchmark tests [1], [2] have been performed, using the devices from several different manufacturers, to check the model’s general applicability and robustness (lack of discontinuities), accuracy, and performance in circuit simulation [18]. We show below some results for the n-channel devices. The MOSFET’s used in the tests are from two different 0.4-μm CMOS technologies with $T_{ox}$ of 9 and 11 nm, respectively, and 3.3-V power supply. The device geometry ranges from 0.4 to 6 μm in channel length, and from 0.6 to 20 μm in channel width. Unless indicated in the figures, symbols represent measured data and solid lines represent the results of the model calculations.

A. Accuracy and Continuity

A set of benchmark tests for the model continuity has been performed and some results are shown in Figs. 3–10 along with the measured data. It can be seen from the different tests that the present model has removed the glitches and negative conductance problems of previous version of BSIM models, and can guarantee the continuities of $I_{ds}$, and its derivatives as well as $G_{m}/I_{ds}$ at all $V_{gs}$ and $V_{ds}$ bias conditions.

The accuracy of the model down to deep-submicron can be seen in Figs. 3–10, where 0.4- and 0.5-μm devices were used. The modeled and measured $I_{ds}$-V$_{ds}$ characteristics are shown in Fig. 3 for the device of $W_{drawn}/L_{drawn} = 20/0.4$ at different $V_{gs}$ bias conditions. It can be seen that in Fig. 3 that the model can fit the measured data well in the whole operation regime, and the maximum relative error is 1.84%. According to the extracted parameter, the effective channel length of the 20/0.4 device is 0.253 μm. It demonstrates that the model can be used to model the characteristics of devices with the channel length down to deep submicron range.

The drain conductance $G_{ds}$ and resistance $R_{out}$ are two important parameters in the analog circuit design. They are shown in Figs. 4 and 5, respectively, for the device of $W_{drawn}/L_{drawn} = 20/0.4$. A very good and smooth fit of $G_{ds}$ can be seen in Fig. 4. Furthermore, in Fig. 5, the model can describe the $R_{out}$ characteristics well in different gate bias conditions, which is a special strength of the BSIM3 model. Besides the general $G_{ds}$-V$_{ds}$ characteristics shown above, SEMATECH also suggested a specific Benchmark called as Gummel symmetry test to test the model continuity [2]. According to the test results obtained by several different companies, the f–V model in BSIM3v3 can pass the Gummel symmetry test [19]–[21]. Because of the length limitation, we do not show the results in this paper.

Figs. 6 and 7 show $I_{ds}$-V$_{gs}$ characteristics of the device of $W_{drawn}/L_{drawn} = 20/0.5$ at $V_{ds} = 50$ mV and different body biases $V_{th}$ in log and linear scale, respectively. A good fit can be observed from the curves between the measured data and model results in both linear and log scales. The maximum relative error is 2.24% in both strong inversion regime and subthreshold regime, which means the model can describe the current characteristics at different bias condition satisfactorily in both subthreshold and strong inversion regimes. Fig. 8 gives the $G_{m}$-V$_{gs}$ characteristics of the device of $W_{drawn}/L_{drawn} = 20/0.4$ at different $V_{ds}$ conditions in both linear and Log scales. The model can match the measured data and ensure a smooth transition from subthreshold to strong inversion regimes again.

As discussed in [1], [2], $G_{m}/I_{ds}$ characteristic of the model is a very important measure to a model used in analog circuit design. It can be seen from Figs. 9 and 10 that the model can guarantee smooth $G_{m}/I_{ds}$ characteristics and fit the data well at different bias conditions.

Besides the model continuity discussed above, it is helpful to the convergence in circuit simulation if the diode model for the source/bulk and drain/bulk junctions can have good continuity. In the BSIM3v3 model implementation, the diode model can ensure the continuities of current and its first directive.

B) Scalability:

To demonstrate the model scalability further, more results for different device sizes are given in Figs. 11–16. Threshold voltage and the saturation current $I_{dsat}$ are two very important parameters in the circuit design and statistical modeling. Figs. 11 and 12 show the measured and modeled threshold voltage characteristics for the devices with different channel lengths and widths. It can be seen that the short-channel and narrow width effects can be well described by the model, at different body bias conditions. The curves of saturation current ($I_{dsat}$) versus device channel length are given in Fig. 13, which shows that the $I_{dsat}$ characteristics can be

---

TABLE I

<table>
<thead>
<tr>
<th>Model</th>
<th>DC time (s)</th>
<th>Total Time (s)</th>
<th>Number of Iterations</th>
<th>DC time (s)</th>
<th>Total Time (s)</th>
<th>Number of Iterations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Level 6</td>
<td>2.4</td>
<td>684.4</td>
<td>16516</td>
<td>8.0</td>
<td>33.7</td>
<td>864</td>
</tr>
<tr>
<td>level 2</td>
<td>14.3</td>
<td>1285.7</td>
<td>16810</td>
<td>16</td>
<td>41.8</td>
<td>449</td>
</tr>
<tr>
<td>level3</td>
<td>1.52</td>
<td>575.0</td>
<td>13077</td>
<td>3.3</td>
<td>21.8</td>
<td>568</td>
</tr>
<tr>
<td>BSIM1</td>
<td>2.25</td>
<td>712.1</td>
<td>16330</td>
<td>4.9</td>
<td>23.4</td>
<td>507</td>
</tr>
<tr>
<td>BSIM2</td>
<td>2.75</td>
<td>872.0</td>
<td>16588</td>
<td>11.0</td>
<td>40.3</td>
<td>703</td>
</tr>
<tr>
<td>BSIM3v2</td>
<td>2.2</td>
<td>728.8</td>
<td>15016</td>
<td>2.15</td>
<td>24.0</td>
<td>578</td>
</tr>
<tr>
<td>BSIM3v3</td>
<td>6.0</td>
<td>1074.8</td>
<td>14119</td>
<td>18</td>
<td>44.7</td>
<td>420</td>
</tr>
</tbody>
</table>
described accurately by the model at different gate biases. In Figs. 14–16, $I_{ds}-V_{ds}$, $I_{db}-V_{gs}$, and $G_{ds}-V_{ds}$ characteristics of devices of different $W/L$ are shown. The maximum error in $I_{ds}$ across different device geometries is less than 5% for the model with one set of parameters.

The BSIM3v3 $I-V$ model has been implemented in some circuit simulators such as Spectre, HSPICE, SmartSpice, and Spice3e2. It has been tested by many users [19]–[21]. The results show that the model is robust and fit the measured data well at wide range of channel lengths and widths for different technologies.

C) Performance Tests:

Many different circuits have been simulated using BSIM3v3. The results of two typical circuits, a 10-bit decoder and a PLL, are shown in Table I. For comparison, the results of other SPICE3 MOSFET models are also included in the table. All simulations are performed with Cadence Spectre [22]. The model is slower than the previous BSIM models due to the more complex model equations. However, the numbers of iterations needed in the simulation is reduced due to the model smoothness, which may lead to easier convergence in complex circuits. Also, the increase in the computation time may be rewarded with the accuracy enhancement in the simulation result. The simulation time may be reduced by future code improvement in the model implementation.

V. CONCLUSIONS

A new physical and continuous BSIM $I-V$ model in BSIM3v3 is presented for MOSFET’s in analog/digital circuit design. The model describes the device current characteristics in all $V_{gs}, V_{ds}$ and $V_{ds}$ condition with a single $I-V$ expression, and guarantees the continuities of current, conductances and their derivatives from subthreshold to strong inversion as well as from the linear to the saturation regimes. The model includes all major physical effects in MOSFET’s. It builds in geometry and process parameter dependence so that it should be superior as a statistical model. The model has been implemented in the circuit simulators such as Spectre, HSPICE, SmartSpice, and Spice3e2.

REFERENCES

Min-Chie Jeng (S’88–M’89) was born in Taiwan, R.O.C. He received the B.S. degree from the National Taiwan University, Taipei, in 1980, the M.S. degree from the University of Maryland, College Park, in 1983, and the Ph.D. degree from the University of California, Berkeley, in 1989, all in electrical engineering. The subject of his master's thesis was the ultra-fast optoelectronic switched and semiconductor lasers. His research for the doctoral dissertation was on the design, characterization, and modeling of deep-submicrometer MOSFET’s.

Since 1989, he has been with Mixed Signal, Cadence Design Systems, San Jose, CA, where he has been working on the development of semiconductor device models for circuit simulators. His other interests include submicrometer MOSFET performance and reliability studies, device characterization, and parameter extraction systems.

Zihong Liu (M’92) was born in Beijing, China. He received the B.Sc. and M.S. degrees in physics from the South China University of Technology in 1978 and 1986, respectively, and the Ph.D. degree in electrical and electronics engineering from the University of Hong Kong in 1990.

From 1990 to 1993, he was with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, as a Postdoctoral Research Fellow and Manager of Device Characterization Laboratory, where his major research activities focused on novel gate oxide preparation and characterization, device modeling, and low-temperature device physics. From 1993 to 1994, he was with Chronet, Inc., San Jose, CA, as a member of the Senior Technical Staff, to develop and implement the BSIM3 model. He has also served as a consultant in several industrial companies. In 1995, he joined BTA Technology, Inc., Santa Clara, CA, taking charge of modeling and characterization tool development, where he is now the President and CEO.

Dr. Liu has published over 50 technical papers and received a Best Paper Award at the 1991 Internal Electron Devices Meeting.

Jianhui Huang, photograph and biography not available at the time of publication.

Mansun Chan received the B.S. degree in electrical engineering (highest honors) and the B.S. degree in computer sciences (highest honors) from the University of California, San Diego, in 1990 and 1991, respectively. He received the M.S. and Ph.D. degrees from the University of California, Berkeley, in 1994 and 1995, respectively. During his undergraduate study, he was working with Rockwell International Laboratory on Heterojunction Bipolar Transistor (HBT) modeling, where he developed the self-heating SPICE model for HBT. His research at UC Berkeley covered a broad area in silicon devices ranging from process development to device design, characterization, and modeling. A major part of his work was on the development of record-breaking SOI technologies. He has also maintained a strong interest in device modeling and circuit simulation. He is one of the major contributors to the unified BSIM3 model for SPICE, which has recently been considered by most U.S. companies and SEMATECH as an industrial standard model. In January 1996, he joined the EEE faculty at Hong Kong University of Science and Technology. His research interests include deep-submicron device technologies, image sensors for single-chip cameras, SOI technologies, high-speed and low-power integrated circuits, device modeling, and automated characterization systems.

Kai Chen (S’88–M’89) received the B.Eng. degree (with honors) from Tsinghua University, Beijing, China, the M.A. degree in physics from Wayne State University, Detroit, MI, and the M.S. degree in electrical engineering from Purdue University, Lafayette, IN, in 1985, 1988, and 1989, respectively. He has been pursuing the Ph.D. degree at the Department of Electrical Engineering and Computer Science, the University of California, Berkeley, since 1992. His current research interests include compact modeling (BSIM3v3), deep submicron MOS device physics, and scaling effects.

Before joining the University of California, he was a Senior Engineer at Fairchild Research Center, National Semiconductor Corporation, Santa Clara, CA, where he worked on yield enhancement and process integration of sub- and half-micron CMOS technology from 1989 to 1992.

Mr. Chen is a Senior Member of the Chinese Institute of Electronics (CIE). He also serves as Executive Committee Member of Northern America Chinese Semiconductor Association (NACSA) and President of Berkeley Chinese Students and Scholars Association (BCSSA). He holds one U.S. patent and has coauthored over 20 research papers.

Ping Keung Ko (S’78–M’81–SM’93–F’96) received the B.S. degree in physics (with special honors) from Hong Kong University in 1974, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 1978 and 1982, respectively. His research interests include high-speed VLSI devices, technology, and circuits; MOS device modeling for circuit simulation; and CAD tools for integrated circuit design.

From 1982 to 1983, he was with Bell Labs, Holmdel, NJ, leading a research team to develop high-speed MOS technologies for communication circuits. He joined the faculty at the University of California, Berkeley, in 1984. He was the Director of the Berkeley Microfabrication Laboratory from 1984 to 1993, and the Vice Chairman of the Department of EECS from 1991 to 1993. He joined UST in August 1993 as a Visiting Professor in the Department of Electrical and Electronic Engineering. Since May 1995, he has been Dean of Engineering.

Professor Ko has authored or coauthored one book and over 200 research papers. His works on MOS technology, MOS device physics, and modeling, and integrated circuit reliability are renowned worldwide. He has extensive experience serving the industrial as well as the professional and academic communities. He was Associate Editor of IEEE TRANSACTIONS ON ELECTRON DEVICES from 1988 to 1990, and was on the program committee of many major international conferences. He has been Chairman of HK Research Grants Council since January 1994, and a member of the UPGC since April 1993.

Cheinning Hu (S’71–M’76–SM’83–F’90) received the B.S. degree from the National Taiwan University, Taipei, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, in 1970 and 1973, respectively.

From 1973 to 1976, he was an Assistant Professor, Massachusetts Institute of Technology, Cambridge. In 1976, he joined the University of California, Berkeley, as Professor of Electrical Engineering and Computer Sciences. While on industrial leave from the university in 1980 and 1981, he was Manager of nonvolatile memory development at National Semiconductor. Since 1973, he has served as a consultant to the electronics industry. He has also been an advisor to many government and educational institutions. His present research areas include VLSI devices, silicon-on-insulator devices, hot electron effects, thin dielectrics, electromigration, circuit reliability simulation, and nonvolatile semiconductor memories.

Dr. Hu is an Honorary Professor of Beijing University, China, and of the Chinese Academy of Science. He has been a guest editor of PROCEEDINGS OF THE IEEE, and of IEEE TRANSACTIONS ON ELECTRON DEVICES. He serves on the editorial board of Semiconductor Science and Technology, Institute of Physics, U.K. He was Board Chairman of East San Francisco Bay Chinese School from 1988 to 1991. He received the 1991 Great News Excellence in Design Award and the 1991 Semiconductor Research Corporation Technical Excellence Award for leading the development of IC reliability simulator, BERT.