Effect of Low and High Temperature Anneal on Process-Induced Damage of Gate Oxide

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Abstract—We have investigated the ability of high and low temperature anneals to repair the gate oxide damage due to simulated electrical stress caused by wafer charging resulting from plasma etching, etc. Even 800°C anneal cannot restore the stability in interface trap generation. Even 900°C anneal cannot repair the deteriorated charge-to-breakdown and oxide charge trapping. As a small consolation, the ineffectiveness of anneal in repairing the process-induced damage allows us to monitor the damages even at the end of the fabrication process.

I. INTRODUCTION

GATE OXIDE damage due to wafer charging processes such as ion implantation and plasma etching has been a major reliability concern for the scaled MOS technology [11–15]. A typical CMOS process usually contains many high-temperature steps which might anneal the damage created by the wafer charging in previous steps. However, the effects of the anneal at different temperatures on the damages have not been studied.

In this paper, we present experimental results on the effect of anneals on stressed oxides. With this knowledge, the damage due to process charging on the end-of-process devices can be estimated.

II. EXPERIMENT

The test structures used are polysilicon gate MOS capacitors with gate oxide thickness of 85Å. No metallization is used and all the probing is done on the polysilicon gates. To simulate the wafer-charging stress, the Fowler–Nordheim stress is carried out at either constant gate voltage or constant gate current. Following the stresses, the wafers are subjected to anneal for 20 min at temperature of 400°C in forming gas (N2/H2) or at temperature of 800°C or 900°C in nitrogen.

Charge-to-breakdown and charge trapping properties are measured on 100 µ2 capacitors using constant injection before and after the anneal. The interface state density is determined by the quasi-static and high-frequency CV measurements on capacitors with areas of 1600µ2.

Manuscript received May 12, 1994; revised August 22, 1994. This work is supported by SRC, Sandia Laboratory, Signetics, TI, Rockwell International and AMD under MICRO program and ISTO/SDIO administered by ONR under contract N00014-92-J-1757.

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Fig. 1. The interface state density (\(D_{it}\)) at mid-bandgap after various stress/anneal conditions. (a) The \(D_{it}\) decay rate after a 400°C anneal. (b) After a 800°C anneal, (c) for anneal at 900°C. The stress is performed with constant voltage on the gate (9 V).

III. RESULT

For devices with relatively lower-level stress (e.g., injection charge less than 20% of charge to breakdown \((Q_{BD})\)), all the interface states created by the stress disappear after the anneal. However, Fig. 1(a) shows subsequent electrical stress can usually bring back about 70% of the interface states created by the original stress but passivated by the 400°C forming gas anneal. This is in agreement with the results reported for damage by plasma etching [6]. Figs. 1(b), (c) show the generating rates of interface states before/after high temperature anneals. For the specific stresses, 900°C anneal is able to remove all the damage and restore the interface to the unstressed status while anneal at 800°C only passivates part of the interface states which re-appear in the subsequent stress.

It is known that oxide charge trapping rate may be studied by observing the rate of rise of the gate voltage under a constant current stress [8]. The shift in the gate voltage \(\Delta V_g\) is related to the trapped charge by \(\Delta V_g = qN_{ox}X/\varepsilon_{ox}\) where \(X\) is the distance of the centroid of the trapped charge from the gate. Fig. 2 shows the charge trapping characteristics of oxides subjected to different charge injection and anneal conditions. After 81s of stress, the oxides are annealed at different temperatures and then subjected to renewed stress until breakdown. Generally, most of the trapped charge can be removed by the anneal as \(\Delta V_g\) goes back to nearly zero after the anneal, however, \(\Delta V_g\) rises quickly after stress is renewed indicating that additional neutral electron traps have been
created during the initial stress and have not been removed by the anneal. The recovering rate of charge trapping depends on the temperature of the anneal. While higher temperature anneal generally removes part of the electron traps created by the original stress, 400°C anneal actually increases the electron trap density slightly.

The data of charge-to-breakdown ($Q_{BD}$) are shown in Fig. 3. For oxides with consecutive stresses without anneal, the total injected charge ($Q_{inj} + Q_{BD}$) is a constant 29 C/cm², as a straight line shown in Fig. 3. For oxide subjected to forming gas anneal at 400°C between the two stresses, the breakdown behavior shows no improvement. Therefore, the usual forming gas anneal has minimum effect on the breakdown characteristics. On the other hand, anneal at 800°C or 900°C improved on the charge-to-breakdown, indicating the partial annealing of whatever oxide damage that is responsible for oxide breakdown. In Fig. 3, after 25 C/cm² of $Q_{inj}$ and 800°C anneal, $Q_{BD}$ is 13 C/cm² corresponding to 16 C/cm² of $Q_{inj}$ without anneal. We conclude that 800°C and 900°C anneals roughly reduce the effective $Q_{inj}$ by 1/3.

IV. DISCUSSION AND SUMMARY

We have studied the effect of high and low temperature anneal in removing the gate oxide damage due to electrical stress on oxide which may be caused by many IC processing steps. The result shows that anneal at 400°C in forming gas removes the stress-induced interface traps and oxide trapped charge but it has no effect in removing the stress-generated neutral electron traps or the damage responsible for breakdown. Even 800°C anneal in nitrogen can only remove about half of interface traps with the other half easily regenerated by after-anneal stress. 800°C anneal has minimal annealing effect on the neutral electron traps. Both 800°C and 900°C anneals can reduce the effect of pre-anneal stress on $Q_{BD}$ by about 1/3, but 900°C anneal can completely anneal out stress-induced interface traps without latent damage and can remove about 15% of the neutral traps.

These results allow us to assess the importance of process-induced oxide damage created prior to high-temperature steps, for example, by source/drain implantation or gate etching, and the damage due to the back-end processes which are followed by only 400°C anneal. To the first order, we can conclude that the effect of process-induced stress on breakdown is cumulative, even with subsequent high-temperature anneals.

REFERENCES