Nanoscale Ultra-Thin-Body Silicon-on-Insulator P-MOSFET with a SiGe/Si Heterostructure Channel

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Abstract—We report the concept and demonstration of a nanoscale ultra-thin-body silicon-on-insulator (SOI) P-channel MOSFET with a Si$_{1-x}$Ge$_x$/Si heterostructure channel. First, a novel lateral solid-phase epitaxy process is employed to form an ultra-thin-body that suppresses the short-channel effects. Negligible threshold voltage roll-off is observed down to a channel length of 50 nm. Second, a selective silicon implant that breaks up the interfacial oxide is shown to facilitate unilateral crystallization to form a single crystalline channel. Third, the incorporation of SiGe in the channel resulted in a 70% enhancement in the drive current.

Index Terms—Heterojunctions, MOSFET’s, SiGe, silicon-on-insulator technology, solid-phase epitaxy, ultra-thin-body.

I. INTRODUCTION

DEVICE scaling has been successfully applied over many CMOS technology generations, resulting in consistent improvement in both device density and performance. However, new challenges are encountered in the scaling of conventional MOSFET structures much below 100 nm. The high channel doping concentration required to suppress the short-channel effect (SCE) results in degraded mobility and enhanced junction leakage. The ultra-thin-body silicon-on-insulator (SOI) MOSFET is a promising structure that suppresses SCE without using a heavily doped channel [1], [2]. With an undoped or lightly doped channel, it also avoids the fluctuation of threshold voltage ($V_{TH}$) due to random fluctuations of the number of dopant atoms in the channel region of nanoscale MOSFET’s [3]. Another attractive approach to improving CMOS performance exploits the strain- or band-structure-induced mobility enhancement to increase the drive current. One of the most notable effects is the enhanced hole mobility in silicon germanium (SiGe) under biaxial compressive strain [4]–[7]. In the sub-100 nm regime, a device that combines the advantages of the SiGe/Si heterostructure and an ultra-thin-body could be the device structure of choice. In this letter, we report the concept and demonstration of nanoscale ultra-thin-body SOI P-channel MOSFET’s and show the enhancement in drive current due to the incorporation of SiGe in the channel.

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Si implant with a dose of $7 \times 10^{15}$ cm$^{-2}$ to break up the interfacial oxide over the source island or over both the source and drain islands, respectively [Fig. 1(b)]. This implant facilitates the crystallization of the amorphous film with the SOI island(s) as the seed. The crystallization step, performed at 550°C for 12 hr, results in lateral solid-phase epitaxy (SPE) growth to form the channel. The range of the lateral SPE is about 0.25 μm. After 20 Å gate oxide growth and in-situ n+ poly-silicon gate deposition, the gate was patterned using electron-beam lithography, and the self-aligned source and drain regions formed by ion implantation [Fig. 1(c)]. Finally, contact-hole etch, metal deposition, and metal patterning steps were performed to complete the device. This device structure is called the SPE MOSFET (SPEFET) [2]. The energy-band diagram of the SiGe-channel SPEFET is shown in Fig. 1(d). The top Si cap layer has a thickness of 40 Å after gate oxide growth. It serves to provide a good Si/SiO$_2$ interface quality. Nearly all of the band-gap difference between Si$_{0.7}$Ge$_{0.3}$ and Si appears at the valence band. As a result, the majority of the holes in P-SPEFET’s are confined in the SiGe-channel, not at the Si/SiO$_2$ interface.

### III. Characterization and Discussion of Results

In Fig. 2, the drain current of the SiGe-channel and the Si-channel P-SPEFET’s are compared. These devices had SPE seeding at the source side only. An enhancement of 70% in the current drive is observed at $V_{DS} = -1.5$ V, $V_{GS} - V_{TH} = -1.2$ V in the SiGe P-SPEFET’s. We believe this is due to the lower effective mass of holes in Si$_{0.7}$Ge$_{0.3}$ which could account for a 20% enhancement and probably the existence of biaxial compressive strain in the channel which lifts the degeneracy of the light-hole (LH) and heavy-hole (HH) bands at the $\Gamma$ point, leading to an even lower in-plane effective mass of the topmost HH band [4], [5]. One speculation on how strain could be incorporated in the SiGe-channel is that the elongated lattice constant of SiGe in the vertical direction gets transferred laterally to the channel region during the SPE growth. Comparable drive currents for the SiGe-channel and Si-channel N-SPEFET’s are observed, and this is expected since the peak electron concentration in the SiGe-channel N-SPEFET biased into inversion is in the unstrained Si cap layer where electron mobility is not enhanced. $I_{DS}$ is low probably due to a large series resistance and further process optimization is needed.

With an unmasked Si implant, the SPE growth proceeds from both ends of the channel and the two growth fronts meet near the middle of the channel, resulting in a low angle grain boundary. With the implant masked such that native oxide is broken up only on one side, crystallization proceeds from one side only, so that the grain boundary in the channel is eliminated at the cost of an additional lithography step. In Fig. 3, the effects of one-and two-sided crystallization on the $I_{DS}-V_{DS}$ characteristics of the SiGe-channel P-SPEFET’s are shown. The elimination of the grain boundary is seen to give about 80% improvement in the drive current at $V_{TH} = -1.5$ V, $V_{GS} - V_{TH} = -1.2$ V. The $I_{DS}-V_{GS}$ characteristics are plotted in Fig. 4 to show the good turn-off behavior of the devices that used one-sided crystallization. Fig. 5 illustrates the excellent short-channel effect of the ultra-thin-body devices. Fig. 4 and 5 also show that the grain boundary not only increases the threshold voltage and sub-threshold swing probably due to the high trap-state density at the grain boundary, but also causes a wider distribution of the $V_{TH}$ values. Fig. 5 also shows that the Si-channel device has 0.2
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Fig. 5. All ultra-thin-body SiGe SPEFET's show little \( V_{TH} \) roll-off down to \( L = 0.05 \mu m \). Both the existence of a grain boundary in the channels due to seeding at source and drain and the larger band-gap in Si-channel device yield high \( V_{TH} \) as expected.

\[ V \text{ higher } V_{TH} \text{ than the SiGe-channel device. This is consistent} \]

with the valence band offset between Si and Si\(_{0.7}\)Ge\(_{0.3}\).

IV. CONCLUSION

In conclusion, we have demonstrated the shortest channel-length (50 nm) SiGe-channel heterostructure MOSFET reported to date. The device has a novel structure that employs an undoped ultra-thin-body on a SOI substrate to suppress the short-channel effects. The thin body is fabricated by lateral SPE which also provides a convenient way to produce the SiGe/Si heterostructure. A 70% enhancement in the drive current is observed due to the introduction of Si\(_{0.7}\)Ge\(_{0.3}\) in the channel. A masked interfacial oxide break-up implant is shown to facilitate unilateral crystallization to eliminate the grain boundary from the channel.

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