The Effect of Channel Hot-Carrier Stressing on Gate-Oxide Integrity in MOSFET's

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Abstract—The correlation between channel hot-carrier stressing and gate-oxide integrity is studied. It is found that channel hot carriers have no detectable effect on gate-oxide integrity even when other parameters (e.g., $\Delta V_f$ and $\Delta I_D$) have become intolerably degraded. In the extreme cases of stressing at $V_G \approx V_f$ with measurable hole injection current, however, the oxide charge to breakdown decreases linearly with the amount of hole fluence injected during the channel hot-hole stressing. This may limit the endurance of a nonvolatile memory using hot holes for erasing. This can also explain the gate-to-drain breakdown of a device biased in the snap-back region, since snap-back at low gate voltage is favorable for hole injection. Snap-back-induced oxide breakdown could be an ESD failure mechanism.

I. INTRODUCTION

THIN gate-oxide wearout is one of the major reliability concerns for MOS integrated circuits. The mechanism of oxide time-dependent breakdown has been attributed to charge trapping [1], [2] or interface state generation [3] in the oxide. Recently, we have demonstrated a close correlation between oxide breakdown and hole trapping with holes generated within the oxide or in the anode electrode by energetic electrons injected via Fowler-Nordheim (F-N) tunneling [4], [5]. One wonders whether externally injected hot carriers (e.g., channel hot carriers) into the oxide would have a similar detrimental effect on oxide integrity. This question is of particular interest to some recent proposals of using hot holes to erase the stored electrons in a nonvolatile memory [6], [7] and also to some applications, e.g., ESD protection device, where snap-back occurs with the gate grounded. If the answer is yes, one further question is the relative importance of oxide wearout versus MOSFET characteristics degradation (e.g., threshold voltage shift) due to hot-carrier stressing. These questions are the motivation for the present work.

Channel hot-carrier stressing, rather than substrate hot-carrier stressing is employed as the carrier injection scheme because of the practical interest mentioned above as well as the versatility of injecting either electrons or holes into the oxide [8], [9], which could also provide some independent evidence regarding the mechanism of oxide breakdown.

II. EXPERIMENT

Silicon-gate n-channel MOSFET's fabricated in three different laboratories were used in this study. The starting materials for the three kinds of devices are boron-doped (100) oriented Si wafers with dopant concentrations of $8 \times 10^{15}$, $7 \times 10^{16}$ cm$^{-3}$, and $2 \times 10^{16}$. The gate oxides for the three wafers were grown in dry oxygen at around 950$^\circ$C to the thicknesses of 200, 90, and 230 Å, respectively. In-situ doped polysilicon was then deposited at 650$^\circ$C and annealed at 900$^\circ$C for 20 min in N$_2$. An LDD structure was fabricated in the third group of devices used where the n$^-$ implant dosage is around $2 \times 10^{11}$ cm$^{-2}$. After source-drain implantation (As, $5 \times 10^{15}$, 120 keV), the wafers were annealed in N$_2$ at 950$^\circ$C for 1 h. The post-metalization sintering was performed in forming gas at 450$^\circ$C for 20 min.

Channel hot-carrier (CHC) stressing was performed at various gate voltages $V_G$ under fixed drain voltage $V_D$ as shown in Fig. 1(a). The threshold voltage shift $\Delta V_f$ as well as the percentage degradation of drain current $\Delta I_D/I_D$ were recorded after the CHC stressing for 1 or 2 h, where $V_f$ is defined as the $V_G$ at which $I_D$ is equal to the channel width-to-length ratio ($W/L$) in microamperes and $\Delta I_D/I_D$ was measured at $V_G = 5$ V with $V_D = 50$ mV for both measurements. After these measurements, the source and drain of the transistor were grounded to the substrate and a constant F-N tunneling current ($I_J = -0.1$ A/cm$^2$) was applied to the gate, as shown in Fig. 1(b), until the destructive breakdown of the gate oxide occurs. The charge to breakdown $Q_{BD}$, defined as $I_J \cdot t_{BD}$ where $t_{BD}$ is the time to breakdown of the oxide, was also recorded as an indication of the oxide integrity after the channel hot-carrier stressing. In this paper, all $I_J$ and $Q_{BD}$ are calculated by dividing current and charge by the area $W \cdot L$, as if the current were uniformly distributed over the gate area. This is done for simplicity (since it is difficult to characterize the actual area of channel hot-carrier injection and the nonuniformity of F-N tunneling current due to the trapped charges) and does not affect the basic conclusion of the study. In the case of snap-back stressing at
low gate voltage, a ramp-voltage $I-V$ measurement follows the stressing, and the breakdown current in the F-N $I-V$ curve is used as a relative indication of oxide integrity.

III. CHANNEL HOT-CARRIER STRESSING WITHOUT SIGNIFICANT HOLE CURRENT

Fig. 2(a) shows the well-known bell-shaped substrate current $I_{SUB}$ and the gate current $I_G$, of a 200-Å gate-oxide transistor with $W/L = 20/2$ (μm) measured at $V_D = 8$ V. The gate current peaking at $V_G = V_D$ is due to channel hot-electron injection into the oxide [8], [9].

Fig. 2(b) and (c) shows the $\Delta V_T$ and $\Delta I_D/I_D$ for such devices stressed at the bias conditions shown in Fig. 2(a) for 1 h. The bell-shaped curves shown in the figures resemble that of the $I_{SUB}$ as expected, supporting the notion that $I_{SUB}$ is a good indicator of the device degradation rate [10]. Because of the severe biasing condition, $V_G$ is less than the minimum snap-back voltage by only 0.5 V, the peak values of $\Delta V_T$ and $\Delta I_D/I_D$ shown in Fig. 2(b) and (c), 100 mV and 8.5 percent, respectively, are beyond the commonly used MOSFET lifetime definition of $\Delta V_T = 10$ mV and $\Delta I_D/I_D = 3$ percent. However, when these severely degraded MOSFET’s were subject to a constant gate current stressing ($I_G = -0.1$ A/cm$^2$) with grounded source-drain, the $Q_{BD}$ values were unchanged as shown in Fig. 2(d), independent of the CHC stressing history. This suggests that, although the channel hot-carrier stressing conditions were harsh, they hardly had any effect on oxide integrity. Parenthetically, this result does not support that the oxide breakdown is due to interface state generation [3], since the stress condition is known to generate a large density of interface traps.

IV. CHANNEL HOT-CARRIER STRESSING WITH SIGNIFICANT HOLE CURRENT

However, for devices operated with a large amount of channel hot-hole injection, the situation is different. In order to create a favorable electric field for hole injection, a high drain voltage ($V_D = 10$ V) was applied to a long n-channel ($W/L = 100/10$ μm) thin-gate-oxide (90-Å) MOSFET. A thin gate oxide is used in this experiment to increase the channel electric field [10] in order to produce large hole current. Because of the high oxide field near the drain when $V_G$ is low, electrons can tunnel from the gate to the drain in addition to the channel hot-hole injection into the gate. The electron tunneling current can be easily measured with the source floating. Fig. 3(a) shows $I_G$ and $I_{SUB}$ as a function of $V_G$ for such a device measured under normal and floating-source conditions. The $I_G$ curve with a peak at $V_G = 0.8$ V is under normal operation, while the other $I_G$ curve, monotonically decreasing with $V_G$, is for the floating-source condition. The difference between these two cases is the contribution of channel hot-hole injection. Fig. 3(b) shows the same $I_G$ versus $V_G$ curves plotted in an absolute scale. The additional $I_G$ curve increasing with $V_G$ from $V_G \approx 6$ V is due to electron tunneling and/or injection from the source or channel into the gate. This gate current component has an opposite sign compared to the other two gate current curves and thus is not shown in Fig. 3(a). Fig. 3(c) shows the $Q_{BD}$ of the devices after channel hot-carrier stressing for 2 h. The small $Q_{BD}$ and the large variation is due to the inferior oxide quality compared to the devices shown in Fig. 2. However, there is a quite apparent drop in $Q_{BD}$ at $V_G = 1$ V where hole injection is most efficient. If the envelope of the $Q_{BD}$ shown in Fig. 3(c) represents the intrinsic breakdown of the devices, then the low values of $Q_{BD}$ after channel hot-carrier stressing at $V_G = 1$ V where the hole current peaks in Fig. 3(a) support the correlation of hole current and oxide breakdown observed in other experiments [4], [5]. This correlation can also be demonstrated by plotting the $Q_{BD}$ data shown in Fig. 3(c) as a function of hole fluence $Q_{hole}$, which is obtained by integrating the gate current density with time during the channel hot-carrier stressing, as shown in Fig. 3(d). In this figure, all the $Q_{BD}$ data fall within a triangle region bounded by a line joining $Q_{BD} = 5$ C/cm$^2$ and $Q_{hole} = 0.08$ C/cm$^2$. This upper bound represents the effect of hole injection on intrinsic oxide integrity. All the other $Q_{BD}$ data falling below the line are due to oxide defect to begin with. A similar experiment, i.e., CHC stressing at fixed $V_G$ and $V_D$ for various amounts of time, can also produce this result. Fig. 3(e) shows the $Q_{hole}$ as a function of CHC stressing time at $V_G = 1$ V and $V_D = 10$ V, and Fig. 3(f) shows
Fig. 2. (a) The well-known bell-shaped $I_{ds}$ and $I_D$ of an n-channel MOSFET measured as a function of $V_G$ with $V_D$ fixed at 8 V. The oxide thickness and $W/L$ of the device are 200 Å and 20/2 μm, respectively. The $I_D$ peaked at $V_G = V_D$ is due to channel hot-electron injection, while the hot-hole injection current is below the detection limit. (b) Threshold voltage shift $\Delta V_T$ versus $V_G$ for devices stressed under the bias condition shown in (a) for 1 h. The peak value of $\Delta V_T$ is around 100 mV, which is much larger than the usual 10-mV lifetime definition. (c) Drain current degradation $\Delta I_D/I_D$ as a function of $V_D$ after the same stressing. The peak $\Delta I_D/I_D$ value, 8.5 percent, is also much larger than the commonly used 3-percent lifetime definition. (d) Charge-to-breakdown $Q_{bd}$ under a constant gate current ($J_G = -0.1 \text{ A/cm}^2$) stressing for devices having experienced the channel hot-carrier stressing shown in (a)-(c). The nearly constant $Q_{bd}$'s suggest oxide integrity is not influenced by the channel hot-carrier stressing shown in (a).

Fig. 3. (a) The $I_D$ and $I_{ds}$ for a thin-oxide (90 Å) long-channel ($W/L = 100/10$ μm) MOSFET measured as a function of $V_G$ at $V_D = 10$ V. The gate current with a peak at $V_G = 0.8$ V is measured under grounded source (normal) condition, while the other $I_D$ is measured with source floated. The difference between these two cases is due to channel hot-hole injection. (b) The same $I_D$ versus $V_G$ curve as in (a) plotted in an absolute value scale. The $I_D$ curve increasing with $V_G$ from $V_D = 6$ V is due to electron tunneling/injection from source–channel into the gate, which has an opposite current sign and thus not shown in the previous figure. (c) $Q_{bd}$ data for the devices after having been stressed under the bias condition shown in (a) for 2 h. The scattering in $Q_{bd}$ data is probably due to sample variations. However, no device shows high $Q_{bd}$ value at $V_G = 1$ V, where hole injection is most efficient. (d) Replot the $Q_{bd}$ data shown in (c) in terms of the hole fluence $Q_{hole}$ integrated during the channel hot-carrier stressing. That all the $Q_{bd}$ data fall within a triangle region suggests a linear correlation between hole fluence and $Q_{bd}$. (e) Hole fluence $Q_{hole}$ as a function of time under the CHC stressing at $V_D = 1$ V and $V_D = 10$ V as shown in (a). (f) $Q_{bd}$ data as a function of $Q_{hole}$ after the stressing shown in (e). A similar triangle region to the one shown in (d) further supports the correlation between oxide breakdown and hole fluence.
the $Q_{bd}$ measured afterward as a function of the hole fluence injected. The similarity between Fig. 3(d) and (f) further supports the correlation of hole fluence and oxide breakdown.

Fig 3(d) and (f) seems to set a stringent constraint on the number of hot-hole erasures a nonvolatile memory cell can withstand. However, if each erasure requires a few times of $10^{-6}$ C/cm$^2$ of holes and the effect of each erasure is additive, then according to Fig. 3(d) the number of hot-hole erasures can be as high as a few times of $10^4$ cycles, which is quite sufficient for many applications.

V. SNAP-BACK INDUCED GATE-TO-DRAIN BREAKDOWN

It has been reported that when a MOSFET is biased into the snap-back region, destructive gate oxide breakdown can occur between the gate and the drain [11]. This is a reliability concern for the ESD at the output devices and input protection circuits where MOSFET’s are driven into snap-back by high-voltage pulses. Since channel hot-hole injection is more favorable at low gate voltages (holes are attracted to the gate), we thus suspect that the snap-back-induced gate-to-drain breakdown could also result from hot-hole injection.

Fig. 4(a) shows the $I_G$ and $I_D$ of a 230-Å gate oxide LDD device ($W/L = 5/3$) as a function of $V_D$ under ground-source (normal) or floating-source conditions. ($V_G = 0.5$ V). Under normal condition, snap-back occurs at $V_D = 19.5$ V, which is manifested by the sudden increase of $I_G$ and $I_D$. The floating-source measurement confirms that the $I_G$ in the snap-back is not due to electron tunneling from gate to drain. (b) The drain voltage $V_D$ and gate current $I_G$ as a function of time during a constant snap-back current stressing of $I_D = 10^{-4}$ A. (c) The F-N tunneling I-V curves of a fresh device and a device experienced the previous snap-back stressing. The crossing of the stressed I-V curve and the fresh one at $I_D = 3 \times 10^{-3}$ A is due to electron trap generation [12]. The oxide integrity degradation for the stressed device is evidenced by the lowering of breakdown current. (d) Breakdown current $I_{bd}$ in the previous ramp-voltage I-V measurement as a function of hole fluence $Q_{hol}$ injected during the stressing. The decreasing of $I_{bd}$ with $Q_{hol}$ once again demonstrates the correlation of hole fluence and oxide breakdown. (e) The same sweep $V_D$ experiment as (a) applied to a shorter channel ($W/L = 5/1.2$) device. Unlike the $W/L = 5/3$ device, there is no directly measurable hole current and thus no instantaneous gate oxide breakdown for the $5/1.2$ device at snap-back. This supports hole injection is an essential factor to degrade the gate oxide.
of snap-back. Fig. 4(b) shows the time evolution of $V_D$ and $I_D$ under stress in this snap-back condition. The gradual increase of drain voltage necessary to maintain a constant snap-back current of $10^{-4}$ A is due to hole trapping in the oxide near the drain in the well-known manner of "walk-out." The decrease of gate hole current with time is also due to hole trapping, which retards further hole injection. Eventually the gate current becomes unstable and starts to rise and the drain voltage starts to fall. The stressing is stopped at this point. Fig. 4(c) compares the F-N tunneling $I-V$ curve of the device after the snap-back stressing to that of a fresh device. The $I-V$ curve for the stressed device begins to the left of the fresh one, crosses the fresh device curve at about $I_G = 3 \times 10^{-12}$ A, and eventually becomes parallel to the fresh $I-V$ curve indicating net electron traps are generated. This however, is as expected since it is known that electron traps can be generated by recombination of holes and electrons in the oxide [12]. The relatively large recombination, and thus trap generation, capture cross section (about $10^{-14}$ cm$^2$) can explain the low current at which those two $I-V$ curves cross (Fig. 4(c)). The parallel $I-V$ shift to the right of the fresh one is either due to trapped electrons or simply due to a reduced charge-free area near the source side. The final current in the $I-V$ curves before breakdown $I_{BB}$ is also lower for devices with snap-back stress, which again indicates that the gate oxide integrity is degraded. Fig. 4(d) shows $I_{BB}$ as a function of the hole fluence injected during the snap-back stress $Q_{hole}$. The fact that $I_{BB}$ decreases with increasing $Q_{hole}$ once again supports that hole injection degrades gate oxide integrity.

Fig. 4(e) shows other supporting evidence that it is hole injection instead of other effects accompanying the snap-back breakdown that degrades the oxide integrity. In this figure, a similar $I_D$ versus $V_D$ experiment as shown in Fig. 4(a) is applied to a shorter channel ($W/L = 5/1.2$) device. The corresponding snap-back breakdown occurs at around $V_D = 15$ V where there is no directly measurable hole current (there is a significant amount of hole trapping, though) and the no instantaneous gate oxide breakdown like the $W/L = 5/3$ device. If any mechanism other than hole injection destroys the gate oxide of the $W/L = 5/3$ device at snap-back, one would expect similar damage to the gate oxide of the $5/1.2$ device.

VI. Summary

The effects of channel hot-carrier stressing on gate-oxide integrity results from channel hot-hole injection. Device stressing without directly measurable hole current, such as typical channel hot-carrier (CHC) stressing, has no significant effect on oxide integrity, despite the large $\Delta V_T$ and $\Delta I_D/I_D$ degradation resulting from the CHC stressing. However, for thin-gate-oxide devices operated at $V_G \approx V_T$ and very high $V_D$, large gate hole current may be observed, and there is a linear correlation between the hole fluence during the CHC stressing and the oxide charge to breakdown measured afterward. For every 0.01 C/cm$^2$ of hole fluence, $Q_{BB}$ is reduced by about 1 C/cm$^2$.

The maximum hole fluence a MOSFET can withstand before the oxide breakdown was found to be about two orders of magnitude smaller than the F-N tunneling electron fluence that the gate oxide can withstand. The snap-back-induced gate-to-drain breakdown observed in ESD protection devices [11] can also be explained by this model. For stressing in the snap-back regime, we have also found a linear correlation between hole fluence and $Q_{BB}$—stressing in the snap-back regime can cause oxide breakdown in a short time because the field condition in grounded gate snap-back is highly favorable for hole injection currents. These results support the belief that oxide breakdown is caused by hole flow and perhaps trapping instead of interface state generation or electron trapping since, without a significant amount of hole fluence, $Q_{BB}$ is independent of $\Delta V_T$ or $\Delta I_D/I_D$, which are generally believed to be associated with interface-state generation or electron trapping. Oxide integrity degradation should not be a concern under the usual hot-carrier-stressing condition where $I_{SUB}$ is at maximum.

REFERENCES


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