The EEPROM as an Analog Memory Device
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Abstract—Nonvolatile storage, electrical programming, and erasing of analog signals have been shown possible for EEPROM’s. Analog signals are sampled, then stored in a commercial 2k×8 EEPROM and read out in a manner simulating speech recording. Modification of peripheral circuitry will make EEPROM’s potential analog memory devices.

I. INTRODUCTION

In previous studies, analog signals have been programmed into MNOS memory cells through the photo-emission process and erased by majority-carrier tunneling [1], [2]. Today, the floating-gate EEPROM is the dominant electrostatically erasable nonvolatile memory technology. The operation of the EEPROM shown in Fig. 1 relies on electron tunneling through a thin oxide [3]. Applying a sufficiently high voltage to the control gate and grounding the drain terminal will make electrons tunnel from the drain to the floating gate, while grounding the control gate and applying a sufficiently high voltage to the drain terminal will lead electrons to tunnel from the floating gate to the drain. Such bidirectional transport enables electrons to be stored on or removed from the floating gate and causes the threshold voltage of the control gate to shift. The magnitude of the threshold shift depends on the number of electrons removed from or added to the floating gate. This can be achieved by changing the write voltage at the control gate or the write pulse width. For commercial EEPROM’s, the write voltage and pulse width are specified so that the sensing amplifier can have enough noise margin to distinguish high and low states. The intermediate levels between high and low states are avoided. However, these intermediate states can be easily attained and used for analog memory applications such as speech recording.

II. EXPERIMENT

Experiments were carried out on a National Semiconductor NMC2816, a 2k×8 EEPROM. A special feature of the NMC2816 is that it provides direct access to the memory cells and bypasses the sensing circuit and output buffers. As described by Yaron et al. [5], by holding the CE pin at 20 V and the Vpp pin at 5 V, the eight I/O pins are directly connected to the drains of eight EEPROM cells. Cell current can be measured by inserting a current meter between the Vcc and I/O pins. The analog signal, therefore, is read in the form of current. The write/erase voltage Vpp is directly applied to the Vpp pin during the write/erase operations. The logic states at the I/O pins distinguish the write and erase operation.

In Fig. 2, we plot the cell read current versus writing Vpp with the CE pulse width as a parameter. To the first order, the cell current increases linearly with Vpp, in agreement with the linear relationship between Vt (Vth of the memory cell on the control gate) and Vpp [4]. Based on this linearity, we decided to use a fixed write pulse width (10 ms) and vary the voltage at the Vpp pin according to the analog signal to achieve fast programming.

Fig. 3(a), (b), and (c) shows the output waveforms of a square, triangular, and sinusoidal waves, respectively. The waveforms are read out at IOH, IOI, and I/O2 pins, respectively, by toggling the address. The original signal is sampled and then programmed into the successive bits of EEPROM memory array. The programming is done by varying Vpp according to the sampled signal. The square wave, the high level of the output waveform is not uniform among the 20 output points shown in Fig. 3(a). The variation results from the nonuniformity of the EEPROM cells. The spikes in the output waveforms are caused by the frequency response of the operational amplifier used in the I/V conversion circuit.

III. DISCUSSIONS

Today’s EEPROM’s can have a writing speed as fast as 0.1 ms. With changes in the write circuit, the write rate can be better than 10K samples per second because many cells can be written individually controlled write voltages simultaneously during a write cycle. This is sufficient for real-time speech recording, for example.
The high voltage for writing can be generated on chip as is routinely done for EEPROM's. The analog signal can be amplified or superimposed on a dc signal and then fed into the charge-pumping circuit to make $V_{PD}$ varying with the input signal. This will, of course, require a high-voltage generator that can supply large current if the design is intended for a single low-voltage supply. Analog sensing can be performed on chip. In the actual circuit that we have built, the cell current is converted to voltage by connecting a resistor between $V_{CE}$ and the I/O pins.

It would be advantageous to store and read the analog signal in the form of $V_i$, (cell threshold voltage) rather than $I_P$. This is because there is an excellent linear relationship between $V_i$ and the WRITE voltage[4]. $V_i$ is expected to be less sensitive to process variations, such as channel length variation, and less sensitive to temperature than $I_P$. Also, this can completely eliminate the $I-V$ conversion procedure. Another advantage of storing and reading signals in the form of $V_i$ is that the input signal can be superimposed on a dc signal and then programmed into the cell. A small input signal is thus stored in a cell that has a high enough $V_i$ to withstand possible signal fading due to charge loss. The higher the input signal is, the larger the cell $V_i$ and hence the number of electrons on the floating gate are. This relieves the limitation due to charge loss and improves signal retention. Charge loss can impose a limit on the minimum voltage that can be stored.

The temperature dependence of $V_i$ will make the magnitude of the readout signal vary with temperature if the analog signal is stored and read in the form of $V_i$. The temperature dependence can be eliminated by comparing the $V_i$ of the programmed cell with that of a reference cell. The accuracy of such a differential sensing scheme is limited by the $V_i$ variation across the memory array. For the storage of a small analog signal, tight control of the $V_i$ distribution is highly desired.

IV. CONCLUSION

The feasibility of using EEPROM's as analog memory devices has been demonstrated with a commercial EEPROM chip. Direct analog storage and readout not only reduce the memory size but also eliminate the need for A/D and D/A conversion. With an EEPROM cell size around 50 $\mu$m, high-density analog storage should be possible. The programming circuit can be integrated easily with fast electrical WRITE/CLEAR capability. There could be potential applications in speech recording or signal recognition.

REFERENCES


Vertical Scalability of Forward Delay Times in Bipolar Transistors

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Abstract—Analytical expressions for the emitter and base forward delay times of a bipolar transistor are derived. The delay times are written in terms of a set of integrals, which allow the dependence on vertical device dimensions to be explicitly stated. These integrals are related to the heavy doping parameters and are valid for arbitrary base and emitter profiles. Simple analytical equations incorporating these integrals can then be used to calculate the delay times.

I. INTRODUCTION

As bipolar devices are scaled to submicrometer geometries, the vertical dimensions of both the emitter and base layers become important in determining the current gain and the quasi-static forward

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