Hot-Carrier Current Modeling and Device Degradation in Surface-Channel p-MOSFET's

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Abstract—The channel field and substrate current models developed for n-MOSFET's are applicable to p-MOSFET's. The impact ionization rate extracted for holes is found to be \(8 \times 10^9 \exp(-3.7 \times 10^6/E)\), where \(E\) is the electric field. Using the lucky electron approach, the gate current of surface-channel (SC) p-MOSFET's has been successfully modeled. Device degradation in p-MOSFET's is due to trapped electrons in the oxide. p-MOSFET lifetime has good correlation with gate current in SC p-MOSFET's. The correlation is better than with substrate current. \(J_i\) can be larger in a buried-channel (BC) p-MOSFET than in a comparable SC n-MOSFET. This makes the SC-MOSFET a much more reliable device. Device lifetime of a p-MOSFET under pulse stress can be predicted from dc stress data for inverter-like waveforms. For other waveforms, there is an extra degradation probably caused by the excess hot carriers generated during the gate turn-off transient.

I. INTRODUCTION

MOST of the studies about hot-carriers effects concentrated on n-MOSFET's rather than p-MOSFET's simply because hot-carrier-induced problems are more serious in n-MOSFET's due to the longer mean-free path, hence higher energy of electrons. For example, peak substrate current in n-MOSFET's is about 3 to 4 orders larger than in p-MOSFET's. In near-micrometer CMOS integrated circuits, n-MOSFET's are known to fail earlier than p-MOSFET's.

For submicrometer or deep-submicrometer CMOS circuits, the hot-carrier reliability of p-MOSFET becomes increasingly uncertain and has drawn considerable attention [1]-[10]. Although under the same bias, there are fewer hot carriers in p-MOSFET's than in n-MOSFET's, they may create different kinds of device instabilities which degrade small-dimension p-MOSFET's rapidly [3]-[6], [9]. In the following, a substrate current model, a model for hot-carrier-induced degradation, and a gate current model in p-MOSFET's are presented. A comparison of degradation characteristics between n- and p-MOSFET's and pulse stress in p-MOSFET's are also discussed.

Our test devices are non-LDD MOSFET's. Both surface-channel (SC) and buried-channel (BC) p-MOSFET's are used. The SC p-MOSFET's are \(n^+\) polysilicon-gate MOSFET's fabricated on n-type substrate without threshold adjust implant. The substrate doping is \(4 \times 10^{19} \text{ cm}^{-3}\). The BC p-MOSFET's are also \(n^+\) polysilicon-gate MOSFET's but fabricated with a n-well CMOS technology and with channel and punchthrough implants performed to achieve desired threshold and punchthrough voltages.

II. SUBSTRATE CURRENT MODEL

It has been shown that for conventional n-MOSFET's the maximum lateral channel field at the drain end \(E_m\) can be expressed in terms of drain voltage \(V_D\) as [11]-[13]

\[
E_m = \sqrt{\frac{(V_D - V_D\text{ SAT})}{l}} + E_{\text{SAT}} = \frac{V_D - V_D\text{ SAT}}{l}
\]

\[
l = 0.22 \tau_{\alpha}^{0.33} X_j^{0.5}
\]

where \(E_{\text{SAT}}\) is the channel field at which the carriers reach saturation velocity. The corresponding drain voltage is \(V_D\text{ SAT}\). \(T_{\alpha}\) is the gate oxide thickness and \(X_j\) is the source/drain junction depth. \(E_{\text{SAT}}\) is about \(4 \times 10^4 \text{ V/cm}\) for n-MOSFET's. As described in [14], \(V_D\text{ SAT}\) can be determined experimentally. Using this relationship, substrate current \(I_{\text{SUB}}\) can be expressed as

\[
I_{\text{SUB}} = \frac{I_D A_e E_m l}{B_i} \exp(-B_i/E_m)
\]

where \(A_e\) and \(B_i\) are the constants in the expression for impact ionization rate, i.e., \(A = A_e \exp(-B_i/E)\), and \(I_D\) is the drain current. Equations (1)-(3) can be shown applicable to p-MOSFET's by plotting \(\ln(I_{\text{SUB}}/(I_D(V_D - V_D\text{ SAT})))\) versus \(1/(V_D - V_D\text{ SAT})\) for p-MOSFET's using experimentally determined \(V_D\text{ SAT}\) [14]. A straight line is obtained as shown in Fig. 1 for different bias conditions and device dimensions using \(E_{\text{SAT}} = 1.2 \times 10^8 \text{ V/cm}\). The result obtained from n-MOSFET's is also included in the same figure. The experimental \(V_D\text{ SAT}\) are

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found to fit a physical expression [13]

\[ V_{DSAT} = \left| \frac{\left( V_G - V_s \right) E_{SAT} R_{eff}}{V_G - V_s} + E_{SAT} R_{eff} \right| \]  

very well. Using (2) for \( L, A, \) and \( B \), deduced from Fig. 1 are

n-MOSFET: \( B_i = 1.7 \times 10^6 \) \( \text{V} \cdot \text{cm}^{-1} \),

\( A_i = 2 \times 10^6 \) \( \text{cm}^{-1} \),

p-MOSFET: \( B_i = 3.7 \times 10^6 \) \( \text{V} \cdot \text{cm}^{-1} \),

\( A_i = 8 \times 10^6 \) \( \text{cm}^{-1} \).

\( B_i \) of the p-MOSFET's is 2.2 times that of the n-MOSFET's, implying that p-MOSFET's can take about twice the \( V_D - V_{DSAT} \) to generate the same \( I_{SUB} \) as n-MOSFET's. As a result, hot-carrier-induced breakdown voltage of a p-MOSFET is also about two times larger [15].

Equations (1)–(4) must be modified for buried-channel p-MOSFET's just as for buried-channel n-MOSFET's [16]. The doping concentration and depth of the buried layer also play important roles in determining the maximum channel field \( E_m \). At low \( V_G \), the buried layer is depleted and can be viewed as an additional insulation layer which gives the buried-channel p-MOSFET an effectively thicker gate oxide. The substrate current of a buried-channel p-MOSFET is thus smaller than that of a comparable surface-channel p-MOSFET [9].

III. CORRELATION OF DEVICE DEGRADATION WITH SUBSTRATE AND GATE CURRENTS

For n-MOSFET's, \( I_{SUB} \) (or \( I_{SUB}/I_D \)) is a well-accepted monitor for hot-carrier-induced degradation, such as \( \Delta V_t \), \( \Delta G_m \), and \( \Delta I_D/I_D \). Device degradation in n-MOSFET's does not appear to have a distinct correlation with gate current. The hot-carrier-limited device lifetime \( \tau \) usually shows a power law dependence on \( I_{SUB} \) (or \( I_{SUB}/I_D \)). The excellent correlation between lifetime and \( I_{SUB} \) is useful for extrapolating n-MOSFET lifetime test data to determine the lifetime at power supply voltage.

For p-MOSFET's, different authors have reported a correlation with \( I_{SUB} \) [6] or \( I_G \) [7], [17]. Fig. 2(a) and (b) shows \( \Delta V_t, \Delta I_D/I_D, I_G, \) and \( I_{SUB} \) versus the stress gate voltage for an SC and a BC p-MOSFET, respectively. For the SC p-MOSFET, the dc stress time is 50 min. The stress condition is \( V_D = -7.5 \) V with \( V_G \) ranging from \(-1\) to \(-6\) V. For the BC p-MOSFET, the stress condition is \( V_D = -10 \) V with \( V_G \) ranging from \(-1\) to \(-6\) V. The dc stress time is also 50 min. \( V_G \) is defined as the gate voltage at which \( I_G = W/L \times 1 \mu \text{A} \) with \( V_D = -50 \) mV. \( \Delta I_D/I_D \) is evaluated at \( V_G = -5 \) V and \( V_D = -0.2 \) V. Notice that \( \Delta V_t \) and \( \Delta I_D/I_D \) are both positive in Fig. 2(a) and (b), independent of the channel type. As can be seen, \( \Delta I_D/I_D \) and \( \Delta V_t \) follow \( I_G \) better than \( I_{SUB} \). No obvious correlation between these two parameters and \( I_{SUB} \) is found. This is different from the case in n-MOSFET's. However, one can still find small humps in both \( \Delta V_t \) and \( \Delta I_D/I_D \) curves near the \( I_{SUB} \) peak in Fig. 2(a) (1-\( \mu \text{m} \) SC p-MOSFET's). The same result is also observed in 432-\( \text{Å} \) SC p-MOSFET's fabricated with the same process.

\( \Delta I_D, \Delta G_m, \) and \( \Delta V_t \) of p-MOSFET's are always positive for the stress conditions stated above. In n-MOSFET's, \( \Delta V_t \) is observed to be positive as well but the transconductance change is negative after stress. These results indicate the presence of trapped negative charges in both cases. The negative charges can be trapped electrons in the oxide and/or acceptor type interface traps. The acceptor type interface traps are negatively charged when occupied by electrons and neutral when unoccupied. In n-MOSFET's the electron density is high, causing the acceptor type interface traps to be occupied and negatively charged. Therefore, degradation of n-MOSFET's can be caused by both trapped electrons in the oxide and acceptor type interface traps. In a p-MOSFET channel, the electron density is very small, most of the acceptor type interface traps are neutral and have no effects on \( V_t \) and \( I_D \).

This explains the observation that a large density of hotcarrier-generated interface traps can be detected by the charge pumping technique but not by a \( \Delta V_t \) [9], [10] or \( \Delta I_D \) measurement. As a consequence, the changes of \( V_t \) and \( I_D \) are mainly due to trapped electrons in the oxide.

Another reason for the dominance of electron trapping in p-MOSFET's is that the vertical field is favorable for electron injection into the oxide. This is consistent with the results in Fig. 2(a) and (b) which show that \( \Delta I_D/I_D \) and \( \Delta V_t \) follow \( I_G \). The small humps in the \( \Delta I_D/I_D \) and \( \Delta V_t \) curves have been interpreted as the effect of interface traps [7]. However, a high density of negatively charged interface traps is unlikely to exist in p-MOSFET's (biased in the linear region) as explained above. An alternative interpretation is that the small humps are also due to trapped electrons in the oxide. The peak of the \( I_{SUB} \) curve corresponds with a peak in the number of hot holes with sufficient energy to create impact ionization. Although this
The above discussion suggests that device degradation should correlate with $I_G$. Fig. 3(a) and (b) shows the device lifetime $\tau$ versus $I_G$ and $I_{SUB}$ for SC p-MOSFET's with 432 and 160 Å gate oxides, respectively. $\tau$ is defined as the time at which $\Delta I_D/I_D$ reaches a certain percentage (2–4%). Devices were stressed with fixed $V_T$ and varying $V_G$. In both cases, the correlation can be expressed as $\tau \propto I_G^m$ with $m = 1.5$. The correlation of $\tau$ with $I_{SUB}$ needs to be fitted with two lines, one for high $V_G$'s and one for low $V_G$'s. For the BC p-MOSFET’s in Fig. 2(b), the correlation with $I_{SUB}$ or $I_G$ is $V_G$-dependent as shown in Fig. 3(c).

During stress, the time dependences of $I_D$, $I_{SUB}$, and $I_G$ were also recorded. On a linear-linear scale, the gate currents always show a rapid decay within the first 1 or 2 min, then gradually settle down. So do the substrate currents, but the relative rates of decrease are much smaller. Both currents do show continuous decay when plotted on a log-log scale. The decreases of $I_G$ and $I_{SUB}$ are caused by trapped electrons in the oxide, which decrease $V_T$ and therefore the channel field through $V_{D,SAT}$ (in (4)). The gate and substrate currents in Figs. 2(a) and (b) and 3(a)–(c) are the values recorded at $t = 0$. The reason to plot lifetime versus initial gate and substrate currents is that the dependence on hot-carrier currents can then be translated into the dependence on channel and oxide fields of the device. We also plot $I_{SUB} \times \tau$ versus $I_{SUB}/I_D$ [4] for the devices in Fig. 3(a). The result is shown in Fig. 3(d). The shape of the curves is similar to that of n-MOSFET’s reported by Choi et al. [20]. This indicates that the oxide field also plays an important role in p-MOSFET degradation, consistent with the result that degradation correlates with $I_G$ better.

The increasing rate of $\Delta I_D/I_D$ with stress-time becomes small after extended stress. Extrapolating the short-term stress data to obtain device lifetimes can introduce large errors. To avoid this, we stress the devices long enough so that $\Delta I_D/I_D$ exceeds or nearly reaches the lifetime criteria.

IV. SHORT-CHANNEL EFFECTS

In both SC and BC p-MOSFET’s, as discussed above, hot-carrier stress causes the magnitude of threshold voltage to decrease and the drain current to increase, leading to circuit drift. A smaller magnitude of $V_T$ means a larger subthreshold current at $V_G = 0$ V and less noise margin for turn-off [5]. Another related parameter is the punch-through voltage $V_{PT}$ [5]. Fig. 4 shows $V_{PT}$ versus stress time for an SC p-MOSFET. Trapped electrons in the oxide, figuratively speaking, turn off the channel near the drain, shorten the channel, and increase drain-induced barrier lowering. The effective “channel shortening” [5], [8] can qualitatively explain the increase in $I_D$, the decrease in $V_T$, and the increase in subthreshold current. In current CMOS technology, BC p-MOSFET’s are widely used. They often have marginally acceptable subthreshold swings and punchthrough voltages. Long-term stress can render them unacceptable. Lightly doped
drain (LDD) and surface-channel (SC) structures will be better alternatives for future deep-submicrometer p-MOSFET's. LDD can reduce channel field and SC p-MOSFET's have better subthreshold swings and punchthrough voltages.

V. GATE CURRENT MODEL

Since gate current is a better monitor than substrate current for device degradation in p-MOSFET's, modeling of gate current is important. Unlike n-MOSFET's, p-MOSFET's exhibit the largest gate current when biased in the saturation region at low $V_G$. The gate current of p-MOSFET's results from electron rather than hole injection into the oxide because electrons have a longer mean free path. Also, the Si–SiO$_2$ barrier height is lower for electrons and the vertical field at low $V_G$ favors electron

Fig. 4. Punchthrough voltage $V_{PVT}$ versus stress time. SC p-MOSFET. $V_{PVT}$ is defined for $V_G = 0$ V, $I_D = I_s = 1$ nA.
injection. Since p-MOSFET’s can take twice as large channel field as n-MOSFET’s before breakdown [15], electron gate current can be higher in p-MOSFET’s than in n-MOSFET’s despite the fact that the number of electrons in p-MOSFET’s, created by impact ionization, is several orders of magnitude smaller than in n-MOSFET’s. Based on the lucky electron model [21], an electron in the channel will eventually reach the gate if 1) it can acquire enough energy from the channel field to surmount the Si-SiO₂ energy barrier, and 2) it does not suffer an energy-stripping collision in the silicon bulk and in the “image potential well” where the oxide field opposes the injection of electrons. Since the source of electrons in p-MOSFET’s is from impact-ionization process which produces electron current \( I_{\text{SUB}} \), the gate current can be expressed as [21]

\[
I_{\text{GATE}} = 0.5 I_{\text{SUB}} \frac{T_{\text{oX}}}{\lambda_e} \left( \frac{\lambda E_{\text{oX}}}{\Phi_b} \right)^2 P(E_{\text{oX}}) \exp \left( -\frac{\Phi_b}{E_{\text{oX}}} \right).
\]  

\[ P(E_{\text{oX}}) \] is the lumped probability that an electron does not suffer an energy-stripping collision per unit length in the silicon bulk and the oxide. The same expression of \( P(E_{\text{oX}}) \) as in [21] is used. \( \lambda_e = 616 \, \text{Å} \) is the redirection scattering mean free path and \( \exp \left( -\frac{\Phi_b}{E_{\text{oX}}} \right) \) is the probability that an electron possesses energy larger than \( \Phi_b \) in a field of \( E_{\text{oX}} \). \( \lambda = 105 \, \text{Å} \) is the scattering mean free path of electrons. \( \Phi_b = 3.2, -2.6 \times 10^{-4} \sqrt{E_{\text{oX}}} - 4 \times 10^{-3} E_{\text{oX}}^{3/2} \) (in volts) is the Si-SiO₂ barrier height considering image force barrier lowering and electron tunneling [22].

\[
E_{\text{oX}} = \frac{V_G - V_D - V_{FB}}{T_{\text{oX}}}
\]

with \( V_{FB} \) being the flat-band voltage. Equation (5) differs from the n-MOSFET expression [21] only in \( I_{\text{SUB}} \) replacing \( I_D \). \( I_{\text{SUB}} \) and \( E_{\text{oX}} \) are calculated from (1)-(4). \( I_G \)'s calculated by this simple model are shown in Fig. 5(a) and (b). The reasonable agreement between the measurement data and calculated values demonstrates the validity of lucky electron model in SC p-MOSFET’s. BC p-MOSFET’s, on the other hand, often exhibit higher gate current than SC devices of the same size [9]. This is due to the difference in flat-band voltage.

The difference in \( I_G \) thus favors p⁺ poly-gate or metal-gate SC p-MOSFET’s over n⁺ poly-gate BC devices for hot-carrier reliability. Another advantage of p⁺ poly-gate p-MOSFET’s is the smaller off-state drain leakage current due to band-to-band tunneling [23].

Fig. 6 shows \( I_{\text{SUB}} \) and \( I_G \) of an n-MOSFET and a p-MOSFET (both are n⁺ poly-gates). The devices are fabricated on the same substrate using an n-well CMOS technology. As can be seen, at the same \( V_D \), the peak \( I_{\text{SUB}} \) of p-MOSFET is about 2 orders smaller than that of n-MOSFET because hole temperature is much lower than electron temperature due to \( \lambda_e > \lambda_n \). However, the peak \( I_G \) of BC p-MOSFET is larger than that of SC n-MOSFET by about 1 order.

VI. COMPARISON OF POST-STRESS I-V CHARACTERISTICS OF n- AND p-MOSFET’S

There is yet no strong agreement on whether degradation mechanism of n-MOSFET’s is mainly interface-trap
generation [24]-[27] or electron trapping [18]. For p-MOSFET’s, the change of device characteristics is generally believed to be caused by charge trapping in the oxide [11]-[5], [8] although interface trap generation also has been considered as an auxiliary mechanism [7], [9]-[10]. By comparing the behaviors of stressed n and p devices, one may be able to gain some insights of the degradation mechanism in n- and p-MOSFET’s.

n-MOSFET’s and p-MOSFET’s exhibit different $I_D-V_D$ characteristics after stress. Fig. 7(a) and (b) shows the forward- and reverse-mode I-V characteristics of an n-MOSFET and a BC p-MOSFET before and after stress. For the n-MOSFET in the forward mode, the saturation drain current of the degraded device approaches that of the fresh device as the drain voltage increases; i.e., the output resistance (ac output resistance, $\Delta V_D/\Delta I_D$) is reduced after stress. On the other hand, the output resistance remains roughly the same for the reverse mode. For the p-MOSFET in the forward mode, the output resistance is less degraded after stress. Furthermore, the post-stress I-V characteristics are more symmetrical than those of the n-MOSFET. The same kind of result as Fig. 7(b) is also observed in SC p-MOSFET’s.

The difference between post-stress I-V characteristics of n- and p-MOSFET’s is explainable in terms of the different properties of interface traps and trapped electrons in the oxide. The charge state of interface traps depends on the Fermi level in silicon. Only charged interface traps and trapped electrons in the oxide can influence the transport of carriers in the channel; neutral interface traps have no effects on the carriers. Since $\Delta V_D$ is positive in both n- and p-MOSFET after stress, it can be concluded that acceptor type interface traps and/or trapped electrons are generated during stress.

For n-MOSFET’s in the linear region, electrons in the inversion layer of n-MOSFET’s charge up the acceptor-type interface traps. Since both trapped electrons and negatively charged interface traps cause $I_D$ and $V_D$ to change in the same direction, their effects on the I-V characteristics of n-MOSFET’s are indistinguishable.

For p-MOSFET’s in the linear region, the density of electrons in the inversion layer is extremely small, the acceptor-type interface traps, if they exist, would be mostly unchanged and have little effects on $V_D$ and I-V characteristics. Therefore, only trapped electrons in the oxide cause the device parameters to change in p-MOSFET’s.

For n-MOSFET’s biased with $V_D > V_G$ in the saturation region, the electron current path in the “pinchoff” region where the interface traps are located is quite deep below the interface. Electron concentration at the interface is low and decreases as $V_D$ increases. Consequently, the percentage of interface traps that are charged becomes smaller and the drain current approaches that of the fresh device. The output resistance of n-MOSFET’s is therefore degraded. One may argue that trapped electrons in the oxide can also explain the low output resistance. The effects of trapped electrons on drain current gradually diminishes with increasing $V_D$ because the effect of trapped electrons is screened out as the channel region over which they reside is depleted.) The turn-on of the source junction due to the increased substrate current after stress in n-MOSFET’s suggested in [28] is not responsible for the degraded output resistance. The post-stress substrate current at point $A$ in Fig. 7(a) is only about 8 nA, which is much too small to forward-bias the source junction and yet the degradation of output resistance is already quite significant.

In the reverse mode, since the acceptor type interface traps at the damaged side (source side) are all charged up, the number of electrons in the inversion layer and the mobility near the source region are greatly reduced. Consi-
sequently, the reduction of drain current is larger for the reverse mode, especially in the saturation region.

For p-MOSFET's in the saturation region, the number of electrons (created by impact ionization) near the interface is even smaller than that in n-MOSFET's; the acceptor type interface traps thus remain neutral and the increase of $I_D$ is mainly due to trapped electrons in the oxide. Since the charge state of trapped electrons in the oxide does not depend on whether the trapped electrons are on the source or the drain side, the forward- and reverse-mode post-stress $I-V$ characteristics are more alike for p-MOSFET's.

VII. PULSE STRESS

Significant difference between ac and dc hot-carrier stress results has been reported for n-MOSFET's [29], [30]. AC stress creates more, or at least equal, damage than dc stress [29]-[32]. The mechanism for the extra damage under ac stress is still not well understood. A proposed mechanism is the interaction between trapped holes and hot electrons [29], [30], [33].

Fig. 8(a) shows $\Delta V_f$ and $\Delta I_D/I_D$ of an n-MOSFET under low- and high $V_G$ stressing. The device was stressed with low $V_G$ and high $V_G$ alternately for four cycles. As can be seen, degradation rate is enhanced after each low $V_G$ stress. Since hole gate current has been observed in n-MOSFET's at low $V_G$ [26], the enhancement in degradation is believed to be caused by the interaction between holes and electrons. Hole injection can lead to trapped holes in the oxides. Once these trapped holes recombine with electrons (injected during high $V_G$ stress), interface traps and/or neutral electron traps [18], [19], [34] can be generated and degradation is aggravated. For p-MOSFET's, however, high $V_G$ stress (favoring hole injection) followed by low $V_G$ stress (favoring electron injection) does not produce the same result as shown in Fig. 8(b). $\Delta V_f$ and $\Delta I_D/I_D$ become saturated as the high-low $V_G$ stress proceeds. The increase of $|V_f|$ and decrease of $I_D$ after high $V_G$ stress are caused by interface trap generation [9], [10], perhaps donor-type [2], [10], and small hole trapping in the oxide. High $V_G$ stress also can cause de-trapping of trapped electrons which are introduced during low $V_G$ stress [35]. The difference between n- and p-MOSFET's may be due to that hole injection in p-MOSFET's at high $V_G$ is much smaller than n-MOSFET's at low $V_G$. No measurable hole gate current has been reported for p-MOSFET's under any bias condition so far. Therefore, no additional neutral traps and/or interface traps are created, and $\Delta V_f$ and $\Delta I_D/I_D$ are not enhanced in p-MOSFET's. This eliminates a possible cause of enhanced ac degradation in p-MOSFET's.

The lifetime under dc stress $\tau_{DC}$ can be expressed as

$$\tau_{DC} = B I_G^m$$

where $B$ is a constant and $m (=1.5)$ is the slope of the line in Fig. 3(a). The lifetime under ac stress is then calculated by [36]

$$\tau_{AC} = \frac{T}{\int_0^T B^{-1} (I_G(t))^m dt}$$

where $T$ is the period, $I_G(t)$ is the gate current at $t < T$. $I_G(t)$ can be calculated from (5). $\tau_{AC}$'s (at $\Delta I_D/I_D = 4\%$) thus calculated are shown in Fig. 9(a) and (b) for $V_{GL} = -3$ and $-8$ V. The calculated lifetimes agree with measured data very well except for the B-case (bad-case) waveform at $V_{GL} = -8$ V. An explanation for the extra degradation under the B-case waveform for n-MOSFET's is the existence of an excess substrate current generated during the $V_G$ turn-on transient in the presence of high $V_D$ [37]. The same explanation is applicable to p-MOSFET's. The average drain and substrate currents shown in Fig. 10 are obtained by varying the overlap time. Ordinarily, one would expect $I_{SUB}$ to be proportional to $I_D$ because both are proportional to the overlap time. This is indeed true for the G-case (good-case) waveform in Fig. 10. The B-case, however, exhibits an excess substrate current $\Delta I_{SUB}$. Through (5), excess substrate current results in excess gate current and therefore extra degradation. This extra component of $I_{SUB}$ is believed to be due to the discharge of stored channel charge through the very high field region at drain during the $V_G$ turn-on transient in the presence of large $V_D$ (low $V_G$ results in low $V_{D\text{SAT}}$ and hence high $V_D/V_{D\text{SAT}}$ form (1)).

Notice that even for the B-case, the excess substrate current would only contribute a small additional degradation if $V_{GL} = -3$ V because most of degradation occurs during $T_{on}$ when $V_G = V_{GL}$ and only a small amount of channel charge is stored and discharged. This is evident in Fig. 9(b). While for the high $V_{GL}$ case, little degrada-
tion occurs during $T_{on}$ yet a large amount of excess carriers are produced during the $V_D$ turn-off transient. As a result, $T_{ac}$ can be orders of magnitude smaller than the quasi-static model (7) would predict as shown in Fig. 9(b). Fortunately, the B-case waveform is rarely encountered in inverter circuits. Therefore, predicting pulse stress p-MOSFET lifetime from dc stress data should be valid at least below a few megahertz of frequency. At much higher frequencies, some other mechanisms could still cause enhanced ac degradation even for Good-case waveforms.

VIII. CONCLUSION

We have shown that both surface-channel (SC) n- and p-MOSFET's share the same channel field expression as a function of $V_D$, $V_{D, sat}$, and device dimensions. p-MOSFET's can withstand twice the channel field of n-MOSFET's to produce the same $I_{Sub}$ or to forward-bias the source junction to cause breakdown. A BC p-MOSFET can have larger gate current than a comparable SC n-MOSFET (and also larger than a comparable SC p-MOSFET).

Hot-carrier-induced device instability in p-MOSFET's is caused by electron trapping in the oxide. Device lifetime shows a $-1.5$ power law dependence on $I_G$ for SC p-MOSFET's. Buried-channel p-MOSFET's do not exhibit a simple $\tau-I_G$ correlation. Correlation between lifetime and $I_{Sub}$ is poor, although $I_{Sub}$, in addition to $I_G$, seems to influence the degradation rate probably through hole-induced electron trap generation. $I_G$ model derived and proven for n-MOSFET's also applies to SC p-MOSFET's with $I_D$ (source of electrons in n-MOSFET's) being replaced by $I_{Sub}$ (source of electrons in p-MOSFET's).

BC p-MOSFET's are more vulnerable to hot-carrier-induced degradation because its subthreshold current swing, punchthrough voltage, and gate induced drain leakage current may be marginally acceptable to begin with. This will favor the use of LDD devices and/or SC devices for future deep-submicrometer p-MOSFET's. Degradation of p-MOSFET's stressed with inverter-like waveforms can be estimated from dc stress data and a quasi-static model. For the ac stressing waveforms with $V_G$ turn-off transient in the presence of high $V_{Dr}$, more degradation than predicted by the quasi-static model is observed. This extra degradation in p-MOSFET's is probably caused by the excess substrate current (hot carriers) generated by the discharge of stored channel charge through the high field region during $V_G$ turn-off transient.

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REFERENCES


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