

# Relating CMOS Inverter Lifetime to DC Hot-Carrier Lifetime of NMOSFET's

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**Abstract**—Comparison with measured 75-MHz CMOS ring-oscillator speed degradation suggests that quasi-static circuit aging simulations using dc stress data do not underestimate circuit degradation. Roughly speaking, 10-percent degradation in NMOSFET linear current results in only about 1.3-percent increase in CMOS inverter propagation delay. This 10-percent current degradation occurs in an inverter-based circuit over a time that is about six times the MOSFET dc lifetime at maximum  $I_{sub}$  and about 30 times the dc lifetime at maximum  $I_{sub}^3/I_{ds}^2$ .

## I. INTRODUCTION

ACCELERATED dc tests have been used to predict and model MOSFET degradation by hot carriers. This letter provides a pragmatic, albeit incomplete and tentative, answer to an urgent question: how to relate such dc device lifetime to circuit lifetime. There are three issues: 1) how to determine the worst-case dc lifetime of a MOSFET, 2) how to relate the MOSFET dc lifetime to the lifetime of a MOSFET in a circuit, and finally 3) how to relate the MOSFET current degradation  $\Delta I_{ds}/I_{ds0}$  to the change in propagation delay  $\Delta\tau_p/\tau_{p0}$ . These three issues will be addressed in the following sections.

## II. DC MOSFET LIFETIME

Today, device lifetime prediction is commonly done under the assumption that maximum substrate current is the worst case for stressing. The theory of hot-carrier degradation suggests [1]

$$\text{degradation} = \left[ \frac{C_1 I_{sub}^m}{W I_{ds}^{m-1} t} \right]^n \quad (1)$$

where degradation denotes  $\Delta I_{ds}/I_{ds0}$ ,  $\Delta V_{th}$ ,  $\Delta g_m/g_{m0}$ , etc.,  $W$  is the device width,  $n$  is approximately 0.5, and  $m$  is around 3 and varies, as does  $C_1$ , with oxide field ( $V_{gd}$ ) [2], [3]. The degradation is actually related to the degradation driving force  $D = I_{sub}^m / (I_{ds}^{m-1} W)$ . For fixed  $V_{gs}$  and channel length  $L$ ,  $I_{ds} \propto W$  and  $D \propto (I_{sub}/W)^m$ ; therefore  $I_{sub}/W$  correlates well with the degradation rate. One can then plot the logarithm of the device lifetime  $\tau$  versus the logarithm of  $I_{sub}/W$ , and extrapolate to find the dc lifetime for the intended operating voltage, e.g., 5 V, at maximum  $I_{sub}$  (point A in Fig. 1(a) and (b)). Whenever  $I_{ds}$  varies over a large range because  $L$  varies [4] or  $V_{gs}$  varies such as in ac stress-

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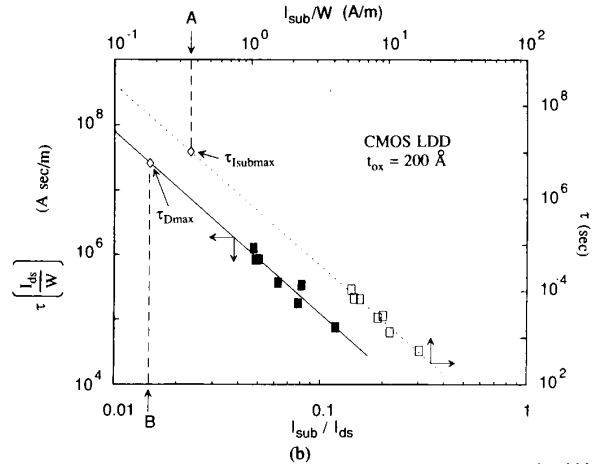
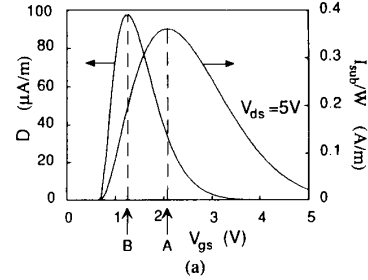


Fig. 1. (a) Degradation driving force  $D$  and substrate current per unit width  $I_{sub}/W$  of an NMOSFET plotted against gate bias. Process is CMOS LDD, with  $t_{ox} = 200 \text{ \AA}$ . (b) Two commonly used methods to extrapolate device lifetime using  $I_{sub}/W$  and  $I_{sub}/I_{ds}$ . Point A corresponds to the lifetime at maximum  $I_{sub}$  for  $V_{dd} = 5 \text{ V}$  (Fig. 1(a)). Point B corresponds to the lifetime at maximum  $D$  for  $V_{dd} = 5 \text{ V}$  (Fig. 1(a)). This lifetime can also be extrapolated by plotting the lifetime measured at maximum  $D$  against  $1/V_{ds}$ .

ing [2], [5], lifetime has been found to correlate well with  $D$  but not with  $I_{sub}/W$ . Fig. 1(a) shows that in this example with  $V_{ds} = 5 \text{ V}$ , maximum  $I_{sub}$  occurs around  $V_{gs} = 2.1 \text{ V}$ , while maximum  $D$  occurs at a lower gate bias, around  $V_{gs} = 1.3 \text{ V}$ . One can determine the worst-case dc stress lifetime at  $V_{ds} = 5 \text{ V}$  by extrapolating the plot of the logarithm of  $\tau(I_{ds}/W)$  measured at peak  $D$  versus  $I_{sub}/I_{ds}$  (point B, Fig. 1(a) and (b)). Lifetime calculated at peak  $D$  (point B) is about five times lower than that calculated at the  $I_{sub}$  peak (point A). Lifetime in Fig. 1(b) is based on 10-percent reduction in  $I_{ds}$  measured at  $V_{gs} = 5 \text{ V}$  and  $V_{ds} = 0.05 \text{ V}$  (hereafter denoted by  $\Delta I_{ds}/I_{ds0}$  unless otherwise noted).

### III. AC LIFETIME AND CIRCUIT AGING SIMULATION

Equation (1), with its parameters determined from dc tests, can easily be modified to calculate degradation for ac stress when  $I_{sub}$  and  $I_{ds}$  are time varying in the so-called quasi-static model [2], [6]:

$$\text{degradation} = \left[ \int \frac{C_1 I_{sub}^m}{W I_{ds}^{m-1}} dt \right]^n \quad (2)$$

with  $C_1$  and  $m$  being functions of  $V_{gd}$  and therefore also time varying [2], [3]. This quasi-static model has been shown to correctly predict ac degradation in the 1-MHz range for inverter-like waveforms [2], [7] and has been implemented in a circuit aging simulator (CAS) [6], which works as a pre- and post-processor to SPICE to simulate the degradation of each NMOSFET in a circuit and the changes in circuit waveforms. There are reports that quasi-static models underestimate ac degradation rates even for inverter-like waveforms at tens of megahertz [5], [8]. These reports either used  $I_{sub}$  rather than  $D$  as the degradation driving force [8] or did not consider  $C_1$  and  $m$  to be functions of  $V_{gd}$  [5]. These omissions are known to cause underestimation of the ac degradation rate [2].

Fig. 2 compares CAS-simulated ring-oscillator degradation with measured data. The 17-stage ring oscillator with 0.25-pF loading at each stage is from a 1- $\mu\text{m}$ , 200- $\text{\AA}$  gate oxide CMOS process using LDD NMOSFET's. Apparently, the measured ring-oscillator period decreases initially because of the increase in PMOS  $I_{ds}$  [9], which was not included in CAS. With this in mind, we conclude that CAS simulated the in-circuit NMOSFET degradation quite accurately. In any event, there is no evidence that properly implemented quasi-static calculation underestimates the degradation of CMOS inverter propagation delay even at 75 MHz.

### IV. RELATING DC LIFETIME TO IN-CIRCUIT MOSFET LIFETIME-DUTY FACTOR

Using CAS, we can relate device-level dc degradation lifetime to device lifetime in a circuit. We have simulated a 16-stage CMOS inverter chain undergoing 5-V operation with a 100-MHz 50-percent duty cycle signal applied at the input. Fig. 3 shows the time required for  $\Delta I_{ds}/I_{ds0}$  of the NMOS transistors in the circuit to equal 10 percent. This is labeled  $\tau_{CAS}$  and is plotted for different capacitive loadings. Also plotted on the same graph are the dc lifetimes extrapolated from maximum  $I_{sub}$  stressing ( $\tau_{Isub\ max}$ ) and from maximum  $D$  stressing ( $\tau_{D\ max}$ ) tests (points *A* and *B* of Fig. 1(b)). The in-circuit MOSFET lifetime,  $\tau_{CAS}$ , is about six times the commonly measured  $\tau_{Isub\ max}$  and 30 times  $\tau_{D\ max}$ . This agrees with the simulated typical duty factor of  $D(t)$  around 3.5 percent.

### V. RELATING $\Delta I_{ds}/I_{ds0}$ TO DEGRADATION OF PROPAGATION DELAY

The inset of Fig. 4 shows the typical  $I_{ds}$ - $V_{ds}$  curves of a fresh and stressed NMOS transistor. Note that the degradation in current is large in the linear region and decreases toward zero at large  $V_{ds}$ . We expect the change in propagation delay

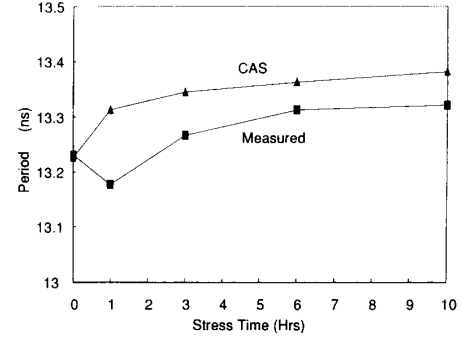


Fig. 2. Measured and CAS-simulated results of oscillation period change of a 17-stage CMOS ring oscillator stressed at  $V_{dd} = 7.5$  V and measured at  $V_{dd} = 5$  V.  $(W/L)_n = (W/L)_p = 20/1.0$  in micrometers. PMOSFET current degradation (increase), not included in the simulation, caused the initial decrease in oscillation period.

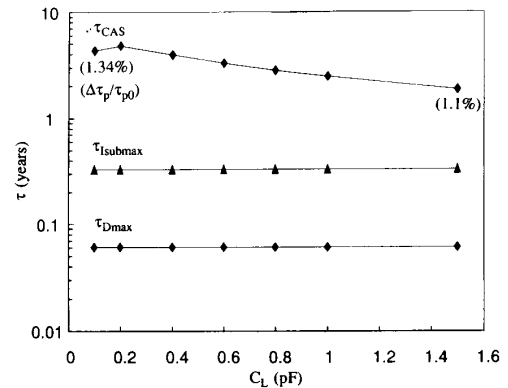


Fig. 3. NMOSFET lifetimes corresponding to a linear drain current degradation of 10 percent plotted against capacitive loading of a CMOS inverter chain.  $V_{dd} = 5$  V, and  $(W/L)_n = (W/L)_p = 20/1.0$  in micrometers.  $\tau_{CAS}$  is the in-circuit device lifetime when the circuit is subject to a 5-V 50-percent duty cycle input at 100 MHz (higher than the maximum clock rate for 1- $\mu\text{m}$  technology).  $\tau_{Isub\ max}$  denotes the dc device lifetime at maximum  $I_{sub}$  (Fig. 1(b), point *A*), while  $\tau_{D\ max}$  denotes the dc device lifetime at maximum  $D$  (Fig. 1(b), point *B*). Note that  $\tau_{Isub\ max}$  and  $\tau_{D\ max}$  are independent of capacitive loading since only one lifetime at points *A* and *B* of Fig. 1(b) is chosen.

to be

$$\frac{\Delta \tau_p}{\tau_{p0}} \approx \frac{1}{2} \frac{\Delta \tau_{fall}}{\tau_{fall}} \approx \frac{1}{4} \left( \frac{\Delta I_{ds}}{I_{ds0}} \right)_{V_{ds}/2} \approx \frac{1}{8} \frac{\Delta I_{ds0}}{I_{ds}} \quad (3)$$

where  $(\Delta I_{ds}/I_{ds0})_{V_{ds}/2}$  is the percentage drain current degradation at  $V_{gs} = 5$  V and  $V_{ds} = V_{dd}/2 = 2.5$  V. The first factor of 1/2 is because the output rise time (pull-up time) is not affected by the NMOSFET and remains unchanged while  $\tau_{fall}$  accounts for about 1/2 of the  $\tau_p$ . The second factor of 1/2 comes from the fact that  $\Delta \tau_{fall}/\tau_{fall}$  is about the average of  $\Delta I_{ds}/I_{ds0}$  at  $V_{ds} = V_{dd}$  (beginning of pull-down,  $\Delta I_{ds} \approx 0$ ) and  $V_{ds} = V_{dd}/2$  (effective completion of pull-down as far as the next inverter stage is concerned). Thus  $\Delta \tau_{fall}/\tau_{fall}$  is half of the percentage current degradation at  $V_{ds} = V_{dd}/2$  (see inset of Fig. 4). Finally, the third factor of 1/2 is because linear region  $\Delta I_{ds}/I_{ds0}$  is about twice the  $\Delta I_{ds}/I_{ds0}$  measured at  $V_{ds} = V_{dd}/2$ .

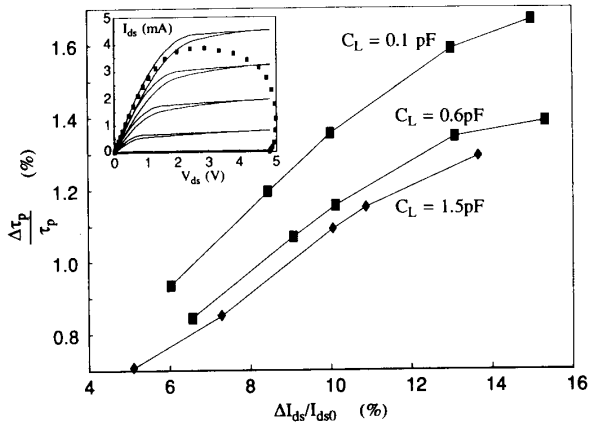


Fig. 4. Simulated inverter chain propagation-delay degradation  $\Delta\tau_p/\tau_{p0}$  plotted against NMOSFET linear current degradation  $\Delta I_{ds}/I_{ds0}$  taken at  $V_{ds} = 0.05$  V and  $V_{gs} = 5$  V. The inset shows the fresh and degraded NMOS  $I$ - $V$  curves plotted with the loci (represented by square symbols) traversed by the NMOSFET during a pull-down transition. The loci of square symbols represents equal time intervals in the transition.

Fig. 4 shows a plot of simulated  $\Delta\tau_p/\tau_{p0}$  versus linear region  $\Delta I_{ds}/I_{ds0}$  for different capacitive loadings. As predicted from the above analysis, every 8 percent of  $\Delta I_{ds}/I_{ds0}$  results in about 1 percent of  $\Delta\tau_p/\tau_{p0}$  in agreement with (3). Finally, the  $\Delta\tau_p/\tau_{p0}$  values shown in Fig. 3, 1.1 to 1.3 percent for 10-percent  $\Delta I_{ds}/I_{ds0}$ , are also in agreement with (3).

#### VI. SUMMARY

As a pragmatic guideline, the following rule of thumb may be taken to estimate the lifetime of an inverter-based circuit from the dc NMOSFET lifetime: propagation delay percentage-wise increases by 1/8 of  $\Delta I_{ds}/I_{ds0}$  (e.g., 10 per-

cent) in six times the NMOSFET dc lifetime (measured at maximum  $I_{sub}$ ). The estimate is believed to be conservative because PMOSFET current increase is not considered and a high clock rate is assumed.

The above is only a rough estimation. More accurate and general circuit aging analysis would require a simulator such as CAS and perhaps a better understanding of the degradation mechanism than is available today. Circuits involving  $V_{gs}$  turn-off in the presence of high  $V_{ds}$  ( $\approx V_{dd}$ ) are subject to enhanced degradation and may not be estimated in the above manner [7].

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