The Reduction of Backgating in GaAs MESFET’s by Impact Ionization

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Abstract—The reduction of drain current due to reverse substrate bias in GaAs MESFET’s fabricated on EL2-compensated substrates is recovered on the application of sufficient drain bias. This recovery is shown to be due to the compensation of the negative space charge at the channel-substrate interface by holes generated by impact ionization in the MESFET channel. Illumination raises the value of drain bias needed for current recovery due to the requirement of additional hole flux to offset the effects of optically generated electrons on EL2 occupancy. Simulation results show that the channel current becomes independent of substrate bias when the bias value is sufficient to completely delete the p-type surface layer.

I. INTRODUCTION

THE undoped LEC semi-insulating (SI) GaAs substrate used in GaAs IC fabrication is obtained by the compensation of residual shallow acceptors by the dominant deep donor-like electron trap EL2 [1]. High-temperature IC processing causes level redistribution, arsenic depletion, and EL2 trap annihilation at the wafer surface, leading to p-type surface layers [2]. These p-type layers and intrinsic trap behavior combine to produce backgating by adjacent electrodes on the surface and by the substrate contact. In this paper, we present experimental data and a simple model to explain the recovery behavior of the MESFET drain current at large drain biases with respect to substrate backgating.

II. EXPERIMENT

Fig. 1 shows the variation of drain current $I_d$ with drain bias $V_d$ (measured in the dark), for different values of substrate bias $V_s$. This tungsten-gate self-aligned device was fabricated on an undoped LEC substrate with nominal gate length $L_g = 1.2 \, \mu m$ and width $W = 10 \, \mu m$. $I_d$ is reduced substantially as $V_s$ becomes more negative, indicating severe backgating. However, $I_d$ becomes independent of $V_s$ for large negative values of $V_s$. As $V_d$ is increased, $I_d$ gradually recovers to the value for $V_s = 0 \, V$ (the top trace). The subthreshold characteristics shown in Fig. 2 show that the threshold voltage ($V_T$) shift saturates at large negative values of $V_s$ with no discernible shift for positive values of $V_s$. Fig. 3 compares the recovery behavior of $I_d$ in the dark with that under microscope illumination, for different values of $V_s$.

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Fig. 1. Recovery of MESFET drain current from substrate backgating on the application of large drain bias with $V_g = V_d = 0 \, V$. The recovery voltage correlates with the onset of significant gate leakage current $I_g$.

III. THEORY AND SIMULATIONS

The inset of Fig. 4 depicts a schematic of the vertical section of a MESFET on an SI substrate with the simulation structure and the doping profile displayed alongside. The p-type layers at the wafer surfaces are created by arsenic outdiffusion and trap annihilation such that the local shallow acceptor density $N_{sa}$ is greater than the local EL2 density $N_{dd}$. $N_{dd}$ is assumed to be constant in the bulk region $y_1$ and modeled to decay exponentially from the bulk value to a lower surface value in the surface regions ($y_2$ at the top and $y_3$ at the bottom). This results in an SI region of thickness $W_{sl}$ and p-type surface layers of thicknesses $W_{sh}$ at the top and $W_{shb}$ at the bottom. The shallow acceptor density is assumed constant for simplicity and the trap level $E_{dd}$ is set to the intrinsic Fermi level $E_F$. The simulations were performed with a two-dimensional simulator [4] modified to include deep-level statistics [5].

The field profiles along a vertical in the simulation structure, for bias values ranging from 0 to 10 V, are shown in Fig. 4. For bias values below 6 V (solid lines), the top n⁺-p junction presents the highest impedance and the applied bias appears directly across this junction leading to backgating.
Once the top p-layer is completely depleted, all additional bias appears across the bottom p-SI junction, which now presents the highest impedance. This is the reason for the saturating behavior apparent in the subthreshold and backgating data shown earlier. $I_d$ becomes independent of $V_b$ for $V_b > 0$ V because the surface p-layer is floating and positive substrate bias merely serves to reverse bias the top p-SI junction, which presents the highest impedance. The macroscopic features of the modulation and saturation mechanisms are not very sensitive to the exact numerical values of the various simulation parameters and the impurity/trap profiles as long as $E_{dd} = E_s$, $N_{dd} > N_{sa}$ in the bulk, $N_{sa} > N_{dd}$ at the surfaces, and the electron capture constant $C_e$ is much greater than the hole capture constant $C_p$.

The recovery behavior for $V_d > 4$ V, also seen in devices with larger gate lengths, occurs along with an increase in the gate current $I_g$ (see Fig. 1). The source current at large $V_d$ ($=7$ V) in the deep subthreshold region ($V_g = -1.2$ V) was a few orders of magnitude smaller than that required for $I_d$ recovery, ruling out DIBL/punchthrough as a recovery mechanism. As pointed out earlier [6], $I_d$ can be used as a monitor of impact ionization in the device channel. The holes generated by impact ionization are partially injected into the substrate and partially collected by the gate. The holes injected into the substrate partially compensate the negative space charge contributed by the ionized shallow acceptors in the depleted surface p-layer, thereby reducing the amount of channel depletion. $I_d$ recovers to the base-line value when all of this negative space charge is compensated. The applied substrate bias is then supported by the bottom p-SI junction. This process is self-limiting since any additional hole injection would increase the local substrate potential beneath the channel and lead to back-injection of holes.

As $V_b$ becomes more negative, the depletion region in the surface p-layer expands, creating additional neutral EL2 traps and negative space charge until the top p-layer is completely depleted. The additional holes that are required for recovery at more negative $V_b$ can only be supplied by additional impact ionization. Thus, the value of $V_d$ at which $I_d$ recovers is larger as $V_b$ becomes more negative. If the supply of holes were purely due to gate Schottky-diode breakdown, then the recovery voltage would exhibit a decrease as $V_b$ is reduced, for the same value of $V_d$. However, the experimental data in Fig. 3 indicate an opposite trend, implying a channel current dependence [6]. The small spread of the recovery voltages is consistent with the model in [6] since the impact ionization current is proportional to the product of the channel current and a multiplication factor, which is exponentially proportional to the negative inverse of the difference ($V_b - V_{d_{sat}}$). For a given $V_d$, the multiplication factor becomes larger as $V_b$ becomes smaller since the drain saturation voltage $V_{d_{sat}}$ tracks $V_d$. However, $I_d$ becomes smaller as $V_b$ is decreased. These opposite trends combine to yield a small recovery voltage spread.

Trap occupancy [5] for the EL2 species is dominated by
the local electron concentration since $C_e$ is over four orders of magnitude greater than $C_p$. Optical illumination, which generates equal concentrations of holes and electrons, shifts trap occupancy to higher values. This makes the local space-charge density ($\rho = q(N_{d0}^+ - N_{d0}^-)$) more negative since the density $N_{d0}^+$ of empty (ionized) EL2 traps decreases. Thus, as in the case of more negative $V_b$, the recovery voltage under illumination shifts to higher values.

IV. CONCLUSIONS

A physical model was presented to account for the annealing of backgating at large values of drain bias. The recovery of the drain current is proposed to be due to the compensation of the negative space charge in the depleted surface p-layer by holes generated by impact ionization in the MESFET channel. Simulation results were presented to show that the saturation of drain current reduction and threshold shift, in response to backgating by reverse substrate bias, are due to punchthrough at the surface p-layer, which limits the peak electric field at the channel–substrate interface. Additional reverse substrate bias merely appears at the p-Si junction near the bottom surface of the substrate. The drain bias at which the drain current recovers is larger under increased reverse substrate bias since a larger hole flux is required to compensate for the additional negative space charge in the p-layer. It is also larger under illumination to offset the effects of the optically generated electrons, which tend to maintain EL2 occupancy at high values. The recovery voltage increases with decreasing gate bias implying that the recovery is not due to breakdown in the gate Schottky diode at large values of $V_{ds}$ but rather due to channel hot electrons.

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