Effect of Hot-Carrier Injection on n- and pMOSFET Gate Oxide Integrity

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Abstract—**N- and pMOSFET's with 9-nm gate oxide are compared. Injected hot holes are found to be about 100 times as effective as electrons in precipitating oxide breakdown. PMOSFET's can tolerate 1000 times more charge injection than nMOSFET's, but not more drain current stress.**

I. Introduction

PREVIOUS works have documented a decrease in charge to breakdown (Q_{BD}) in nMOSFET's following hot-carrier injection [1]-[3]. It has been shown that hole injection in nMOSFET's is detrimental to gate oxide integrity. In this paper, that effect is examined quantitatively and pMOSFET's are studied for comparison.

II. Experiment

The devices used for this experiment are abrupt junction MOSFET's with n^+ polysilicon gates. Drawn channel length is 1.2 μm and channel width is 10 μm. The n-channel devices have gate oxide thickness of 9 nm; X_{ox} of the p-channel devices is 8 nm.

A HP 4145 parameter analyzer is used to bias the devices as well as measure voltages and currents; a HP 9836 computer is used to control the experiment. The experiment consists of two parts. First, the gate, source, and substrate are grounded while a fixed amount of drain current is forced to flow. Impact ionization occurs near the drain and the gate–drain potential difference is favorable for injection of holes (electrons) from the nMOSFET (pMOSFET) channel to the gate. Fig. 1 shows the current–voltage characteristics for devices biased in this manner. The amount of charge passing through the oxide is calculated by integrating the gate current with time. This number is converted to charge density (Q_{inj}) by dividing it by the product of the device width and the distance over which hot carriers are injected (estimated to be 0.1 μm [4]). Next, constant (Fowler–Nordheim tunneling) current stress is performed to measure charge to breakdown (Q_{BD}). Electrons are injected from the gate.

III. Charge to Breakdown of NMOSFET's

The nMOSFET $I-V$ characteristics shown in Fig. 1 were generated by ramping the drain current with all other terminals grounded. The rise in drain current when drain voltage exceeds 4 V is due to gate-induced drain leakage (GIDL). As the drain voltage further increases, impact ionization near the drain occurs, eventually leading to snapback. As the figure clearly shows, when an nMOSFET is biased beyond snapback, the device produces gate current in excess of that due to Fowler–Nordheim tunneling of electrons from the gate to the drain. The polarity of drain voltage indicates that this excess current is due to holes injected from the channel to the gate. This hole gate current reduces Q_{BD} as shown in Fig. 2.

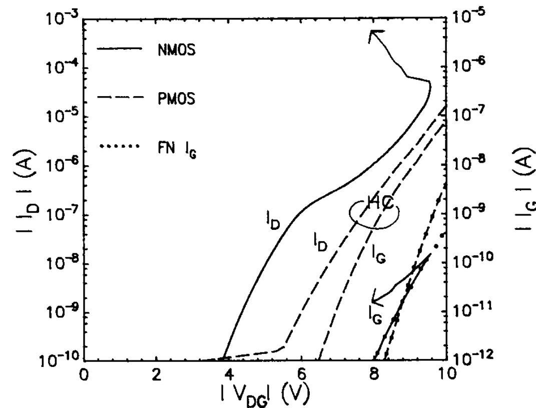

Fig. 1. $I-V$ characteristics for the devices used in this study. NMOS: all terminals except the drain grounded; device dimensions are $L_{eff} = 1.05$ μm, $W = 10$ μm, and $X_{ox} = 9$ nm. Dotted line shows Fowler–Nordheim tunneling current for comparison; this is measured with $V_D = 0$ and $-V_G$ bias. PMOS: "FN" current was generated by biasing the gate and grounding the other terminals; curves labeled "HC" were drawn with all terminals except the drain grounded. Device dimensions are $L_{eff} = 1.2$ μm, $W = 10$ μm, and $X_{ox} = 8$ nm. Gate current generated during hot-carrier stress is much larger in PMOS than in NMOS.

Fig. 2 shows Fowler–Nordheim Q_{BD} as a function of Q_{inj}. Q_{inj} was varied by changing the value of drain current applied for 60 s. Q_{inj} was also varied by adjusting the stress time and fixing the drain current at 0.1 mA; these points are marked in Fig. 2. There is a sudden drop in the value of Q_{BD} when the drain is stressed near or beyond the snapback current. This is coincident with the appearance of the hole component of gate current in Fig. 1.

These data indicate that it takes fewer holes passing through the oxide to cause breakdown than it does electrons. A theory which purports that a critical event leading to oxide wearout is hole trapping [5] can explain these data. Holes can be generated by electrons passing through the oxide or, in the case of stressing in the snapback regime, by hot-hole injection. We expect that Q_{inj}(at $Q_{BD} = 0$)/Q_{BD}(fresh) for the

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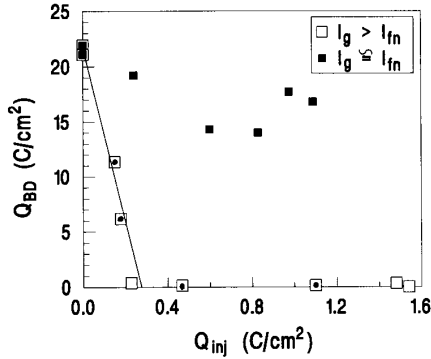

Fig. 2. Q_{BD} between gate and drain is measured following hot-carrier stressing of n-channel transistors. Charge injected during hot-carrier stress is very effective in reducing subsequently measured Q_{BD}. This is attributed to the presence of holes in I_g during hot-carrier stress. The data points marked with dots correspond to stressing at $I_d = 0.1$ mA for varying times.

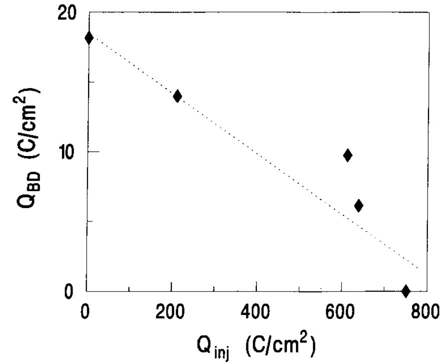

Fig. 3. Q_{BD} between gate and channel is measured following hot-carrier stressing of p-channel transistors. The devices were stressed at $I_d = -10$ μA for various time intervals. Gate current generated during hot-carrier stress is no more effective in creating breakdown than is tunneling gate current.

$I_g > I_{fn}$ case in Fig. 2 is the probability that an electron creates a hole while passing through the oxide. This ratio is approximately 0.01. This value increases with the electric field used during the Q_{BD} test; 10.5 MV/cm was used in this experiment (electric field calculation includes the effects of band bending).

If the devices were biased such that I_g were solely due to electrons, one would expect the slope of Q_{BD} versus Q_{inj} to be approximately 1. However, in Fig. 2, even the data points corresponding to $I_g \cong I_{fn}$ follow a line with slope greater than 1. This is attributed to a small hole component of the current as evidenced by walk-out.

IV. Charge to Breakdown of PMOSFET's

The pMOSFET I_d and I_g curves labeled "HC" in Fig. 1 are generated in the same way as the nMOSFET curves on the same figure. The drain current is due to GIDL and impact ionization. Some of the hot electrons are injected into the oxide and cause the appearance of I_g. The "FN" curve was obtained by ramping V_g with the other terminals grounded. I_g due to hot carriers is much larger than Fowler–Nordheim I_g for the same electric field.

Fig. 3 shows Q_{BD} versus Q_{inj} for p-channel devices. Q_{inj} was varied by changing stress time at a fixed I_d. In contrast with the n-channel device results, hot-carrier gate current is no more, and in fact is less, effective in precipitating breakdown than is tunneling gate current. This result is not surprising because in p-channel devices both types of current are due to electrons. The oxide is seen to withstand more Q_{inj} than Q_{BD}; this is because hot-electron injection occurs at lower oxide field and, therefore, generates fewer holes [6] than do tunneling electrons.

V. The Relation Between Q_{BD} and Stress Current

During an overvoltage event or in a circuit environment, stress is often due to a current source; therefore, it is useful to examine the reduction in Q_{BD} as a function of drain

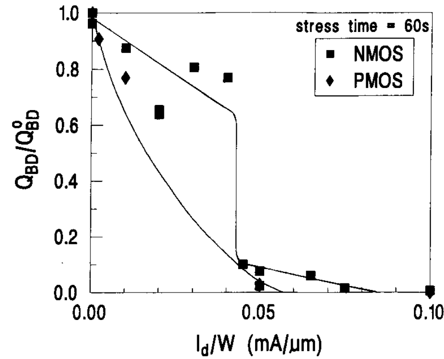

Fig. 4. Q_{BD} decreases with increasing drain current in both n- and p-channel devices, although for different reasons. Solid lines indicate expected results.

current stress as in Fig. 4. N-channel and p-channel device lifetimes are seen to be comparable. This may seem surprising in light of the results presented in Figs. 2 and 3, i.e., p-channel gate current consists of the flow of electrons, which is 100 times less damaging than holes, but may easily be explained. The ratio of I_g/I_d is about three orders of magnitude larger in p-channel devices than in n-channel devices (see Fig. 1), because the mean-free path of electrons is longer than that of holes and the barrier height for injection of electrons from Si into SiO_2 is 1.4 eV lower than that for holes. For a given I_d, a p-channel device will have more I_g than an n-channel device; however, the current will be solely due to electron flow in the p-channel device while there is a hole component of I_g in the n-channel device. The net result is that both drain currents are approximately as effective in reducing Q_{BD}. Of course, a higher voltage was applied to the pMOSFET in order to force a given I_d.

P-channel Q_{BD} decreases as stressing is done at progressively higher I_d for two reasons. First, as I_d increases, so do I_g and Q_{inj}. Fig. 3 shows that Q_{inj} reduces Q_{BD}. The

second factor is the increasing oxide electric field. The charge injected during the hot-carrier stress becomes increasingly effective in leading to breakdown as the electric field increases.

In the n-channel devices, near the onset of snapback the fraction of I_g consisting of holes rises. This causes a steep drop in the value of Q_{BD}.

VI. Conclusions

Holes are about 100 times as effective as electrons at 10.5 MV/cm of oxide field in causing oxide breakdown. Gate current in nMOSFET's under stress conditions is due to holes and electrons; the gate current in pMOSFET's is about 1000 times as large, but solely due to electrons. As a result, the reduction in Q_{BD} after hot-carrier stress at the same I_d is similar in n- and p-channel devices. However, pMOSFET's can tolerate upwards of 1000 times more hot-carrier injection.

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