Bipolar–FET Hybrid-Mode Operation of Quarter-Micrometer SOI MOSFET’s

Stephen A. Parke, Chenming Hu, Fellow, IEEE, and Ping K. Ko, Member, IEEE

Abstract—A “hybrid” mode of device operation, in which both bipolar and MOSFET currents flow simultaneously, has been experimentally investigated using quarter-micrometer channel length MOSFET’s which were fabricated on SIMOX silicon-on-insulator substrates. This mode of device operation is achieved by connecting the gate of a non-fully-depleted SOI MOSFET to the edges of its floating body. Both the maximum $G_a$ and current drive are 1.5 × higher than the MOSFET’s normal mode. BJT-like 60-mV/decade turn-off behavior is also achieved. This mode of operation is very promising for low-voltage, low-power, very high-speed logic, as well as on-chip analog functions.

I. INTRODUCTION

LOW-POWER, high-speed logic is one of the primary motivations for developing deep-submicrometer thin-film SOI technologies. Transistors which have high current drive and high transconductance with a low voltage swing are required. Bipolar ECL logic can achieve high speed at low voltages, but with a large power dissipation. A new low-power solution is the “hybrid-mode” operation of deep-submicrometer SOI MOSFET’s, where both surface-channel and buried bipolar conduction occurs. In this configuration, the gate and floating body of the device are connected at the device edges. This mode of device operation has been studied extensively for bulk MOSFET’s built in individual isolated wells [1]–[4], but it can be implemented more simply and with higher performance on thin-film SOI. Unusually high bipolar current gains (> 10000) are observed in this mode of operation, due to high emitter efficiency. This is the result of electron injection barrier lowering in the depletion region near the top-side gate, while the hole injection barrier from the quasi-neutral base into the emitter is unchanged. This behavior is similar to a heterojunction BJT, leading to high gain and excellent low-temperature characteristics [5]. Hybrid-mode device operation has previously been demonstrated on laser-recrystallized SOI [6]. However, these devices utilized light channel doping, resulting in a low threshold voltage so that the MOSFET was turned on before the BJT. The full advantage of lateral bipolar action was not achieved. In this work, we fabricated NMOS devices on SIMOX substrates with a gate oxide of 8.5 nm and $L_{eff}$ down to 0.2 μm. These devices exhibit high current drive, high $G_a$, and ideal BJT turn-off behavior at low voltages, while exhibiting MOSFET behavior at higher voltages. The floating substrate problems associated with non-fully-depleted SOI MOSFET’s are eliminated as well.

II. THEORY OF OPERATION

The hybrid-mode configuration and location of important device current components are shown in Fig. 1. At subthreshold voltages, bipolar current dominates, with a pure lateral BJT component (3) and a component which is injected over a lowered barrier near the gate and then swept upward toward the oxide interface (2). The latter component actually dominates. On the other hand, the base current is composed primarily of holes injected into the emitter (4). The barrier for these back-injected holes is not lowered by the gate. Therefore, a barrier difference exists between the electron injection region near the surface and the hole injection region in the bulk, resulting in a large emitter efficiency and high current gain. In addition, the $V_{th,em}$ is lowered by approximately 0.3 V, permitting lower switching voltages for these devices. At higher gate voltages, the MOSFET channel current (1) is dominant and most of the injected electrons are swept upward into the channel. Both the transconductance and collector current are superpositions of the MOS and BJT components.

III. DEVICE FABRICATION

The devices were fabricated on SIMOX substrates, with a final SOI thickness of 180 nm. Conventional LOCOS isolation was performed, followed by a 50 keV, 7 × 10¹²/cm² boron threshold implant. An 8.5-nm gate oxide was then grown, and a 300-nm phosphorus in-situ-doped gate was deposited. The resulting devices were non-fully-depleted, with a long channel $V_T = 0.7$ V. Oxygen plasma “ashing” was done to the gate photoresist to achieve effective channel lengths down to 0.2 μm. High-dose arsenic and boron source/drain implants completed the critical processing. The body/base of the transistor is contacted at the device edges by a p⁺ implant, as shown in Fig. 1. A four-terminal layout was used to operate the device in either pure MOSFET, pure lateral BJT, or hybrid mode. The body is either floated or grounded in MOSFET mode. The gate is grounded in lateral BJT mode. The gate and body are connected in hybrid mode.

In addition to this four-terminal layout, devices with local
gate-to-body connections at both device edges were also fabricated, as shown in Fig. 1. This simple connection uses an oversized aluminum-to-p⁺ contact window aligned over a "hole" in the poly gate. Thus, the aluminum shorts the gate and p⁺ regions. This contact requires minimal area and no additional processing steps. All device processing was performed in the UC Berkeley Microfabrication Laboratory.

IV. DEVICE CHARACTERIZATION

Fig. 2 shows the subthreshold behavior of a four-terminal NMOS device in each of its operation modes. This device is interdigitated with \( W = 8 \times 10 \, \mu\text{m} \) and \( L_{\text{eff}} = 0.3 \, \mu\text{m} \). The ground-body NMOS exhibits \( V_{\text{tr}} = 0.7 \) V and \( S = 93 \, \text{mV/decade} \). The grounded-gate n-p-n exhibits a current gain of 15 and a knee current of only 0.5 mA. This poor bipolar performance is due to the relatively long basewidth and small emitter cross section, i.e., high current density. The hybrid mode of operation is superior to both of these, with \( S = 60 \, \text{mV/decade} \). The \( V_{\text{tr}} \) is reduced by 0.3 V, showing the barrier lowering effect of the gate on the collector (electron) current. Thus, the hybrid-mode device turns on at lower voltage than either the MOS or BJT with BJT-like transconductance. Hybrid-mode current gain of over 10,000 was achieved, compared with a gain of 15 for the lateral BJT.

The hybrid-mode device exhibits superior current drive and transconductance. Fig. 3 shows the \( I_{\text{d}}-V_{\text{c}} \) characteristics of the \( L_{\text{eff}} = 0.3 \, \mu\text{m} \) device in each of its operation modes. The BJT current drive is low due to base current crowding and high-level injection in this range of collector current. The floating-body MOS \( I-V \) characteristics exhibit higher current drive, but show the familiar kink. However, the hybrid-mode current drive is \( 1.5 \times \) higher than the MOS, and nearly \( 5 \times \) higher than the lateral BJT, for the same gate voltage. The transconductance of this device in each of the three modes is shown in Fig. 4, for \( V_{\text{c}} = 1.5 \) V. For the BJT mode, \( g_m \) increases from \( V_{\text{bem}} = 0.70 \) V until \( V_{\text{be}} = 0.85 \) V, after which high-current effects cause it to decrease. On the other hand, the MOS \( g_m \) saturates at 215 mS/mm. The hybrid-mode \( g_m \) is bipolar-like at low gate voltages, but reaches a much higher value (340 mS/mm at \( V_{\text{c}} = 0.8 \) V) than the BJT \( g_m \) due to the 0.3-V reduction in \( V_{\text{bem}} \). At higher gate volt-
ages, the hybrid-mode transconductance decreases due to high-level injection and becomes controlled by MOS channel current, dropping to 265 mS/mm at $V_g = 1.5$ V, which is still 25% higher than the MOS-mode $g_m$.

V. CONCLUSIONS

This hybrid-mode operation of short-channel SOI MOSFET's is very promising for sub-1-V, ultralow-power logic, especially due to the reduction in $V_{bnm}$ and the bipolar-like low-voltage behavior. The high gain is also promising for analog applications. Finally, while this operation mode is available in any CMOS technology without any additional processing steps, it is especially suited to thin-film SOI.

REFERENCES