High-Performance Sub-Quarter-Micrometer PMOSFET's on SOI

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Abstract—PMOS transistors with effective channel lengths down to 0.15 µm have been fabricated on silicon-on-insulator (SOI) films. Gate oxide thicknesses of 5.5 and 10 nm are used. These P+ gate PMOS devices exhibit excellent short-channel behavior, low source–drain resistance, and remarkably large current drive and transconductance. For \( T_{ox} = 5.5 \text{ nm} \), saturation transconductances of 274 mS/mm at 300 K and 352 mS/mm at 80 K are achieved, which are the highest reported values for this oxide thickness. The result is attributed to low series resistance, forward-bias body effect, and the reduction of body charge effect.

I. INTRODUCTION

POTENTIAL advantages of MOS transistors built in thin SOI films include less process complexity, reduced parasitic capacitances, improved short channel effects, absence of latch-up, and higher transconductance and current drive. However, to date very few successful experimental results have been reported to substantiate improved current drive. Often high parasitic series resistance has obscured this advantage [1]. Here, for the first time, we report experimental results for deep-submicrometer SOI PMOSFET's with improved performance over their bulk counterparts.

II. DEVICE FABRICATION

A full description of the process integration is given in [2]. Here, we provide only the key processing steps. SIMOX substrates with a final SOI film thickness of 130 nm were used. The 130-nm film thickness permits low device series resistance without using silicidation. Also, by avoiding ultrathin films, desired threshold voltage can be easily achieved. Mesas were created by plasma etching a nitride/oxide/silicon stack stopping at buried oxide. Next a 100-nm oxide was grown on the mesa sidewalls to prevent low-\( V_T \) edge devices and gate oxide defects at the mesa corners. Threshold implants were then performed, resulting in concentrations of \( 1\times 10^{17} \text{ cm}^{-3} \). Gate oxides of 5.5 and 10 nm thickness were grown, followed by the deposition of 280 nm of undoped polysilicon. Doping of the poly gate was realized by a 30-keV 5 x 10\(^{15}\) cm\(^{-2}\) boron implant. The combination of P+ polysilicon, silicon film thickness, and doping concentration resulted in nearly fully depleted (NFD) devices with threshold voltage range of \(-0.3\) to \(-0.5\) V. These threshold voltages are consistent with intended low-voltage operation of the devices. Effective channel lengths as short as 0.08 µm were obtained by O\(_2\) ashing of the gate photoresist [3].

III. DEVICE PERFORMANCE

We note that all reported channel lengths here are the effective channel lengths, determined from standard conductivity measurement, not the mask lengths. Fig. 1 shows the \( I-V \) characteristics of a 9.5-µm/0.2-µm device with \( T_{ox} = 5.5 \text{ nm} \). Although fabricated devices are NFD, and long-channel devices show kink in their \( I-V \), very short devices have reduced kinks as seen in Fig. 1. This is due to the fact that the depletion regions of the source/drain junctions nearly deplete the film at drain voltages lower than the onset of the kink. Fig. 2 shows the subthreshold swing and threshold voltage shift (\( \Delta V_T \)) of the fabricated PMOSFET's. Although ultrathin film is not used, good subthreshold swing and short-channel behavior is observed. Subthreshold characteristics of a device with \( L_{eff} = 0.2 \mu m \) are shown in Fig. 3.

Fig. 4 shows that for \( T_{ox} = 5.5 \text{ nm} \), the device with \( L_{eff} \) of 0.15 µm has saturation transconductances (\( G_m \)) of 274 mS/mm at room temperature and 352 mS/mm at 80 K. These are measured values and have not been corrected.
for series resistance effect. In fact a key to achieved transconductance is the relatively low series resistance, which ranges from 700 to 1100 Ω·μm for our devices. The $G_m$ of our devices with $T_{ox} = 10$ nm is higher than those reported for bulk devices with $T_{ox} = 6$ nm and $T_{ox} = 8$ nm [4], [5]. Fig. 5 similarly shows that the $I_{sat}$ of present devices is larger than recently reported values for both bulk and SOI devices with thinner gate oxides [1], [5], [6].

There are several reasons for SOI devices built on thin silicon films to have higher $G_m$ and $I_{sat}$ over their bulk counterparts. Fully depleted (FD) and nearly fully depleted (NFD) devices have reduced or no bulk charge effect that raises the local $V_f$ increasingly toward the drain. Reduced bulk charge also reduces the local effective vertical field and improves the carrier mobility [7]. An additional effect not reported before is the effect of forward bias on the floating body even before the onset of the kink. To demonstrate this effect, special four-terminal devices with body contacts were fabricated on the same die as regular three-terminal devices. Fig. 6 shows the $I$–$V$ of a four-terminal device. Three sets of curves are shown with body floating, body grounded, and $-0.3$ V (forward bias) applied to the body. $I_f$ is clearly larger with the fourth terminal open than grounded. However, the floating-body case and the forward-bias case match before onset of the kink, indicating that a forward bias of about 0.3 V is present when the body is floating. Since the body–drain junction is reverse biased and some leakage current flows from drain to body, the forward bias of the
body–source junction allows this current to flow from body to source. One drawback of the forward bias is reduction of threshold voltage and increase of leakage current at $V_g = 0$, as seen in Fig. 3.

IV. CONCLUSION

Using SIMOX wafers with silicon film thickness of 130 nm, PMOS transistors with effective channel lengths down to 0.15 $\mu$m are fabricated. These devices exhibit excellent short-channel behavior, low series resistance, and remarkable $G_m$ and $I_{\text{sat}}$. For $T_{\text{ex}} = 5.5$ nm, $G_m$ of 274 mS/mm at 300 K and 352 mS/mm at 80 K are achieved, which are the highest reported values for this oxide thickness. The high performance is attributed to low series resistance, reduction of body charge effect, and the forward-bias body effect.

REFERENCES