Modeling Oxide Thickness Dependence of Charging Damage by Plasma Processing

Hyungchel Shin, Student Member, IEEE, Ko Noguchi, and Chenming Hu, Fellow, IEEE

Abstract—We have developed a quantitative model for thin oxide plasma charging damage by examining the oxide thickness dependence of charging current. The current is deduced from capacitance–voltage (CV) curves of metal-oxide-semiconductor (MOS) capacitors after plasma etch. The model predicts the oxide thickness dependence of plasma charging successfully. It is shown that plasma acting on a very thin oxide during processing may be modeled as essentially a current source. Thus the damage will not be greatly exacerbated as oxide thickness is further reduced in the future. Gate oxide breakdown voltage distribution of MOS capacitors after plasma processing can be predicted accurately from that of a control wafer by using a defect-induced breakdown model.

I. INTRODUCTION

PLASMA processing degrades thin gate oxides today and it lowers the very large scale integration (VLSI) yield [1]–[6]. There is an urgent concern about the effect of plasma processes on future thinner oxide [1]–[4]. What will the effects be devastating? There is no quantitative model to predict the oxide thickness dependence of plasma charging. Although there have been several attempts to model the plasma [7], [8], the effect of plasma processing on the yield of the oxide and the dependence of the oxide thickness is not clear.

In this paper, we present a quantitative model to explain the oxide thickness dependence of plasma charging. With this model, one can predict the effect of plasma processes on future thinner oxides.

II. EXPERIMENT

The test structures used are polysilicon gate MOS capacitors with Al antenna. The gate oxide was thermally grown in dry oxygen at 900 °C. The Al antenna was connected to the polysilicon gate via a contact hole through CVD oxide. The Al etching was done by Cl₂ gas (30 sccm) in a parallel-plate, diode-mode etcher with radio frequency of 13.56 MHz at 250 mtorr and 250 W.

III. RESULTS AND DISCUSSION

The interface trap (D_it) generation caused by Al plasma etching is shown in Fig. 1 for three different oxide thicknesses. ΔD_{it} of the 6.4-nm oxide was not larger but smaller than ΔD_{it} of the thicker 11.6-nm oxide. ΔD_{it} of the 11.6-nm gate oxide was larger than that of 18.0-nm gate oxide. The reason for this gate oxide thickness dependence of ΔD_{it} will be discussed later.

By comparing the CV curve of a capacitor after etching to those after constant-current stress, one can determine the plasma charging current [5]. Fig. 2 shows the deduced plasma charging current and the corresponding oxide voltage and oxide field for three oxide thicknesses. Although the charging current varied by two orders of magnitude, this corresponds to an oxide field variation of only 30%, and the oxide charging voltage is basically proportional to oxide thickness. In this sense, the plasma produces not a fixed-voltage stress, but a more a fixed-field stress. The reduced D_{it} generation in 18.0-nm oxide compared to 11.6-nm oxide shown in Fig. 1 is attributable to a smaller charging current for thicker oxide. The reduced D_{it} generation in 6.4-nm oxide compared to 11.6-nm oxide is due to the well-known greater tolerance of thinner oxides to Fowler–Nordheim (FN) current stress, possibly due to the reduced rate of oxide generation in the thinner oxide [12].

It is useful to understand why the charging current has a thickness dependence. The plasma charging current I_p is composed of steady ion current I_i and pulsed electron current. The net time-average current causes oxide charging [9]. After averaging the plasma charging current over time, the plasma charging current involves a modified Bessel function but can be expressed by the “Langmuir-probe” IV characteristics

\[ I_p = I_i - I_{e0} \exp \left( \frac{eV_g}{kT_e} \right) \]  (1)

where I_{e0} is the magnitude of the electron current at \( V_g \) (antenna voltage) = 0 V [10], [11]. Since this current flows through the oxide as an FN tunneling current, the oxide voltage and hence current is determined from the simultaneous solution of (1) and the FN current equation (2).

\[ I_p = \text{oxide area} \cdot A \left( \frac{V_g}{T_{ox}} \right)^2 \exp \left( -\frac{BT_{ox}}{V_g} \right) \]  (2)

where \( T_{ox} \) is the oxide thickness and \( A = 20 \ \mu A/V^2 \), \( B = 250 \ \text{MV/cm} \) are known constants. Fig. 3 compares
the intersections (solutions) of (1) and (2) with experimentally deduced current and voltage. \( I_e \) can be estimated from the de voltage, sheet thickness, and the exposed antenna area. \( I_{sc} \), 8.2 nA and \( V_r = 4 \) eV [see (1)] can be found from a plot of \( \text{In}(I_e - I_p) \) versus \( V_e \), with \( I_p \) and \( V_p \) from Fig. 2. Since the gate antenna voltage is smaller for the thinner oxide, the plasma charging current is larger. Fig. 3 shows that the charging current in a very thin oxide (\( V_e \rightarrow 0 \) V) remains finite and reasonable. Therefore, for thin oxides, it is better to think of the plasma as an imperfect current source with the current somewhat modified by the gate electrode voltage. Since the ion current is proportional to ion density, reducing the ion density is an effective way to lower the current at low \( V_e \).

Fig. 4 shows the oxide voltage and oxide charging current as a function of oxide thickness calculated from (1) and (2). Experimental values are also shown in the figure. As the gate oxide thickness decreases, the charging current approaches a constant; the ion current, and therefore the corresponding gate voltage is almost proportional to gate oxide thickness in the thin-oxide regime.

We also examined the effect of plasma etching on oxide yield. After plasma etching, more failures were observed in thinner oxides than in thicker oxides (Fig. 5). This is because more charge flows through the thinner oxide (28.5 mC/cm\(^2\) for the 6.4-nm oxide versus 7.75 mC/cm\(^2\) for the 11.6-nm oxide and 0.25 mC/cm\(^2\) for the 18-nm oxide), as shown in Fig. 2. This is also because thinner oxides have more low-\( Q_{BD} \) defects in the starting oxides for a given fabrication environment. \( Q_{BD} \) (and ramp breakdown voltage \( V_B \)) after a certain electrical stress can be predicted by a defect-induced breakdown model [13]. Loosely speaking, oxide breakdown occurs if the charging current and process time product exceeds \( Q_{BD} \). The oxides barely surviving the plasma charging also have slightly reduced \( Q_{BD} \) [13].

IV. SUMMARY

During plasma processing, MOS devices are subjected to electrical stress from plasma, which acts as not a voltage source but an imperfect current source, fortunately for future thinner oxide. The stress on the oxide is roughly equivalent to applying a fixed electric field that is weakly dependent on the gate oxide thickness. Degradation of very thin oxides in terms of \( \Delta D_p \), becomes smaller as the oxide thickness is decreased. Using the initial oxide
Fig. 5. Cumulative failure percentage of MOS capacitors versus ramp breakdown voltage at 0.1 V/s (or charge-to-breakdown). Open symbols are used for Al wet-etched control capacitors, and solid symbols are for Al plasma-etched capacitors. Model prediction after plasma etching shown by broken lines matches the data well.

$Q_{BD}$ data, one can accurately predict the breakdown voltage or charge to breakdown distribution after plasma processing. Lowering the ion density is one of the effective ways of reducing the charging current in the thin oxides.

REFERENCES


