Hot-Carrier Effects in Thin-Film Fully Depleted SOI MOSFET's

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Abstract—Previous conflicting reports concerning fully depleted SOI device hot electron reliability may result from overestimation of channel electric field ($E_m$). Experimental results using SOI MOSFET’s with body contacts indicate that $E_m$ is just a weak function of thin-film SOI thickness ($T_{th}$) and that $E_m$ can be significantly lower than in a bulk device with drain junction depth ($X_j$) comparable to SOI’s $T_{th}$. The theoretical correlation between SOI MOSFET’s gate current and substrate current are experimentally confirmed. This provides a means ($I_G$) of studying $E_m$ in SOI device without body contacts. Thin-film SOI MOSFET’s have better prospects for meeting breakdown voltage and hot-electron reliability requirements than previously thought.

I. INTRODUCTION

THIN-FILM fully-depleted (FD) SOI MOSFET’s have attracted much attention because of their larger drain saturation current, absence of kink effect, and superior sub-threshold leakage. However, as far as device reliability and breakdown voltage are concerned, previous reports are divided on whether FD SOI devices have reduced or enhanced hot-carrier susceptibility and the sensitivity to SOI film thickness [1]-[7]. The main difficulty is that substrate current ($I_{SUB}$), the convenient monitor of channel field for bulk MOS devices, cannot be measured on the conventional SOI devices with floating body. While gate current has been suggested as a lifetime parameter for SOI devices [6], [7], gate current is small, difficult to measure, and sensitive to charge trapping and the vertical field. Gate current characterization cannot be confirmed as a valid monitor of channel field without substrate current. In this study, for the first time, using a special SOI device structure with body contact, both substrate (body) current ($I_{SUB}$) and gate current ($I_G$) were directly measured in the same devices. Based on this experiment, not only is the channel field in SOI devices quantified, but also the correlation between $I_{SUB}$ and $I_G$ is established.

II. EXPERIMENTS

The FD n- and p-channel SOI devices were fabricated on SIMOX wafers using a CMOS process. The buried oxide thickness is about 3500 Å. LOCOS isolation and 3000-Å in-situ doped n+ poly gate were used. To collect $I_{SUB}$, the n-MOS devices have a special p$^+$ region to contact the p-type body. The p$^+$ region was formed by p-MOS S/D implant ($B_{11}$, $4 \times 10^{15}$ cm$^{-2}$, 30 keV). Similarly, p-MOS devices have an n$^+$ region to contact n-type body using n-MOS S/D implant ($A_{S}$, $4 \times 10^{15}$ cm$^{-2}$, 70 keV). The measured $I_{SUB}$ in these structures is found to be proportional to the channel width, indicating the high efficiency in collecting $I_{SUB}$.

III. RESULTS AND DISCUSSIONS

In bulk MOSFET’s, the maximum channel field can be estimated as follows [8]:

$$E_m = (V_D - V_DSAT)/l = (V_D - V_DSAT)/(0.22T_{ox}^{1/3}X_j^{1/2})$$  

(1)

where $l$ is the characteristic length. The hot-carrier currents, $I_{SUB}$ and $I_G$, can be expressed as [9]

$$I_{SUB} = A_t/B_t(V_D - V_DSAT)I_D \exp(-B_t/E_m)$$  

(2)

$$I_G = C(E_{ox})I_D \exp(-\varphi_b/E_m)$$  

(3)

By combining (2) and (3), we get

$$\ln\left(\frac{I_{SUB}}{V_D - V_DSAT}\right) = \ln\left(\frac{A_t}{B_t}\right) - \frac{B_t l}{V_D - V_DSAT}$$  

(4)

$$I_G = \frac{C(E_{ox})B_t}{A_t(V_D - V_DSAT)}\left(\frac{I_{SUB}}{I_D}\right)^{(\varphi_b)/(B_t)}$$  

(5)

where $A_t$ and $B_t$ are known constants for impact ionization rate, i.e., $\alpha = A_t \exp(-B_t/E)$ [9], $\varphi_b$ is the barrier height at Si/SiO$_2$ interface, $\lambda$ is the scattering mean-free path, and all the other parameters have their usual meanings.

In SOI devices, the definition of drain junction depth ($X_j$) is not clear. Colinge used $T_{th}$ to substitute $X_j$ in (1) to estimate the channel field [3], while Chen et al. [6] reported that this overestimates $E_m$. From expression (4), a plot of $\ln(I_{SUB}/(I_D(V_D - V_DSAT)))$ versus $1/(V_D - V_DSAT)$ should yield one straight line for all bias voltages, as shown in Fig. 1. The slope of this straight line gives $B_t l$, from which $l$ and hence $E_m$ can be determined experimentally. It is found
that using thin-film SOI thickness ($T_{si}$) to substitute $X_J$ can overestimate $E_m$ by a factor of 2 (roughly equivalent to overestimating $V_{th}$ by more than 50%).

$I_{SUB}/I_D$ is a simple monitor of the channel filed $E_m$. Figs. 2(a) and (b) show the distribution of measured $I_{SUB}/I_D$ for the SOI and bulk devices, respectively. Although $T_{si}$ variation across a wafer is as high as 200 Å, the $I_{SUB}/I_D$ variation is only ±10% and comparable to the ±10% variation in the bulk case, confirming the weak $E_m$ sensitivity to $T_{si}$. Besides, an SOI device has lower $I_{SUB}/I_D$, and hence $E_m$, by around 400% than the bulk device (see Figs. 2(a) and (b)), although $V_{DSAT}$ are about the same. $T_{si}$ was determined by the CV technique [10].

Both the lower $E_m$ and weaker $E_m$ dependence on $T_{si}$ for SOI devices can be attributed to the lateral drain doping gradient effect in thin-film SOI devices based on 2D simulation [11]. The simulation found relatively low $E_m$ and weak $E_m$ sensitivity on $T_{si}$ within the range of interest (500–1100 Å). $E_m$ is a function of the lateral drain doping gradient even for non-LDD As drains. In the case of bulk MOSFETs, the doping gradient varies with $X_J$; this contributes to the $E_m$ dependence on $X_J$. In the case of SOI MOSFETs, lateral doping gradient is decoupled from $X_J$ (or $T_{si}$). Hence, $E_m$ can be lower in SOI device with small $T_{si}$ than in a bulk device with small $X_J$, and $E_m$ is a weak dependence on $T_{si}$ as well.

Previous reports have been divided on whether FD SOI devices are less [3]–[7], or more [11], [12] vulnerable to hot-carrier effects. The knowledge that FD SOI devices can have a lower channel field $E_m$ than the bulk devices should also be reflected from the device degradation in terms of hot-carrier stress. Fig. 3 shows the lifetime versus $I_{SUB}$ for n-channel SOI and bulk devices under the worst case (maximum $I_{SUB}$) stress conditions. Although $X_J$ for the bulk devices is as large as 2000 Å, the SOI devices with $T_{si}$ = 800 Å are still less

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**Fig. 1.** Experimental determination of the characteristic length $l$ in $E_m = (V_D - V_{DSAT})/l$ in SOI and bulk n-MOS devices. In bulk device, the measured $l$ is 461 Å. In SOI device, the measured $l$ is 1194 and 1254 Å, while the $l$, based on the bulk MOSFET $E_m$ model with $X_J = T_{si}$, are 554 Å and 616 Å, implying that $E_m$ in SOI devices can be much lower than in bulk devices with shallow abrupt drain.

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**Fig. 2.** Distribution of $I_{SUB}/I_D$ of SOI and bulk n-MOS devices. (a) SOI. (b) Bulk n-MOS devices. Both $I_{SUB}$ and $I_D$ were measured at the maximum $I_{SUB}/I_D$ point with $V_D$ = 4 V. The sensitivity to SOI $T_{si}$ is very weak. The variations of $I_{SUB}/I_D$ across both wafers are about ±10%. SOI has lower $I_{SUB}/I_D$ and hence $E_m$ (by around 400%) than the comparable bulk MOSFET.

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**Fig. 3.** Device hot-carrier lifetime versus substrate current for SOI and bulk n-MOS devices. $W_{eff}/L_{eff} = 4.5 / 0.8 \mu m$. Under stress, $V_D = 4.5 - 6.5 V$ with $V_G$ varied so that $I_{SUB}$ can be adjusted. The lifetime $\tau$ is defined as the stress time to reach 10% $\Delta I_D/I_D$. The slope is about $-3.5$. 
MOSFET. The decoupling of SOI MOSFET junction depth \( T_{\text{sil}} \) and lateral doping gradient is a little discussed but significant advantage in drain engineering. The correlation between \( I_{\text{SUB}} \) and \( I_G \) is confirmed and suggests that the channel field may be characterized through the measurable \( I_G \). This realization improves the prospects of thin-film SOI devices meeting breakdown voltage and hot-carrier effects requirements. \( I_G \) measurement should help drain structure design engineering.

REFERENCES


