An Accurate Semi-Empirical Saturation Drain Current Model for LDD N-MOSFET

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Abstract—Based on a new empirical mobility model which is solely dependent on $V_{gs}$, $V_t$, and $T_{ox}$, a corresponding semi-empirical $I_{dsat}$ model for n-MOSFET including velocity saturation, mobility degradation due to increased vertical effective field, and source/drain series resistance of LDD structures is reported in this paper. A good agreement among the model and the measurement data from several different technologies is shown. Prediction of $I_{dsat}$ for the future generations of device scaling and low-power applications by using this new model is presented.

I. INTRODUCTION

Among all MOSFET parameters, saturation drain current $I_{dsat}$ has the strongest impact on circuit speed and is arguably the most important single parameter. Yet, the model is almost universally used to analyze or even predict the effect of gate-oxide thickness, $T_{ox}$, channel length, $L_{eff}$, and voltage supply, $V_{dd}$, on $I_{dsat}$ has been the following one:

$$I_{dsat} = \frac{1}{2} \left( \frac{W_{eff}}{L_{eff}} \right) \mu_{eff} \left( \frac{e_{ox}}{T_{ox}} \right) (V_{gs} - V_t)^2.$$  

(1)

This is very inadequate for today’s MOSFET’s because of the effects of velocity saturation; short-channel effect ($V_t$ “roll-off”); mobility degradation with the increased vertical channel field, $E_{ox}$; and source and drain series resistance of LDD structures, $R_s$ (which represents the series resistance for the source end only in this paper) must be considered.

Starting from an empirical n-MOSFET inversion electron mobility model that is solely dependent on device parameters of $V_t$, $V_{gs}$, and $T_{ox}$, and a derivation of $I_{dsat}$ including $R_s$ of LDD, a corresponding semi-empirical $I_{dsat}$ model for n-MOSFET is presented in this paper. Measurement data of several different technologies are compared with the new model. The power of this new model to predict the trend of $I_{dsat}$ for future technologies as well as low-power applications is demonstrated. It should be noted that this paper does not attempt to model $V_t$ with respect to $L_{eff}$; therefore, in all figures except the last one, the $V_t$ used for the model are the measured values for each respective $L_{eff}$. The use of such measured values of $V_t$($I_{dsat}$) automatically considers the short-channel effect (including DIBL).

II. RESULTS AND DISCUSSIONS

As shown in Fig. 1, the measured mobility of MOSFET’s inversion layer carriers observes the following empirical mobility model [1]:

$$\mu_{eff} \left( \frac{cm^2}{V \cdot s} \right) = \frac{540}{1 + \left( \frac{E_{ox}}{0.9} \right)^{1.85}} = \frac{540}{1 + \left( \frac{V_{gs} - V_t}{0.47 \cdot T_{ox}} \right)^{1.85}}$$

(2)

for NMOS electrons [1]. Here $E_{ox}$ is in the unit of $(MV/cm^2)$. The physical mechanism governing MOSFET’s strong inversion carrier mobility at room temperature is phonon scattering. The ionic scattering becomes dominant at lower $E_{ox}$ (weak inversion to subthreshold regions of MOSFET) as shown in Fig. 1. This deviation from universality at low $E_{ox}$ does not affect the accuracy of the $I_{dsat}$ modeling because MOSFET’s operate at strong inversion when $I_{dsat}$ is modeled. Because the electron mobility degrades with the stronger $E_{ox}$ or smaller $T_{ox}$, event the long-channel $I_{dsat}$ for thin $T_{ox}$ deviates from the relationship of $I_{dsat} \propto \frac{1}{T_{ox}}$ predicted by (1).

In addition to the mobility degradation, the velocity saturation has to be considered for today’s MOSFET’s with relatively short channels [2]:

$$I_{dsat} = W \nu_{sat} C_{ox} (V_{gs} - V_t - V_{dsat})$$

$$= W \nu_{sat} C_{ox} \frac{(V_{gs} - V_t)^2}{V_{gs} - V_t + E_{sat} L_{eff}}$$

(3)

where saturation velocity $\nu_{sat} = 8 \times 10^{6} \text{ cm/s}$, $V_{dsat}$ and $E_{sat} = \frac{V_{dsat}}{L_{eff}}$ are the drain saturation voltage and the electric field corresponding to velocity saturation, respectively. The series resistance at the source end, $R_s$, of the devices characterized for this work are around 20-45 $\Omega$ for $W = 20 \mu$m (or equivalently 400–900 $\Omega$-$\mu$m). These are pretty typical values of practical LDD MOSFET’s. The effective gate bias is reduced more than 0.2 V from $(V_{gs} - V_t)$ to $(V_{gs} - V_t - I_{dsat} R_s)$. Hence the effect of $R_s$ can be neglected for the MOSFET’s with LDD. For the purpose of accounting for $R_s$, (3) can be rewritten as:

$$I_{dsat} = W \nu_{sat} C_{ox} \frac{(V_{gs} - V_t - I_{dsat} R_s)^2}{V_{gs} - V_t - I_{dsat} R_s + E_{sat} L_{eff}}.$$  

(4)
Fig. 1. New universal electron mobility in terms of \( V_{gs}, V_{t}, \) and \( T_{ox} \); three technologies with three body bias for each are shown. \( V_{sat} (i = 1, 2, \text{and } 3) \) indicates the zero-body bias-threshold voltage for each technology, respectively.

Solving for \( I_{dsat} \) from this quadratic equation, the \( I_{dsat} \) function expressed explicitly in terms of \( R_s \) and other parameters is obtained in (5), as shown at the bottom of the page, where \( V_t = (V_{gs} - V_t) + E_{sat} L_{eff}. \) The first order Taylor expansion of (5) leads to the following approximation for \( I_{dsat}(R_s) \) for LDD MOSFET's in general:

\[
I_{dsat}(R_s) = I_{dsat0} \left( 1 - \frac{2I_{dsat0} R_s}{V_{gs} - V_t} + \frac{I_{dsat0} R_s}{V_{gs} - V_t + E_{sat} L_{eff}} \right)
\]

(6)

where \( I_{dsat0} = I_{dsat} (R_s = 0) \) is given by (3). When the measured values of \( V_t, L_{eff}, \) and \( R_s \) are used, the calculated \( I_{dsat} \) from (5) or (6) is plotted against the measured \( I_{dsat} \) in Fig. 2. The short-channel effect (including the DIBL effect) is thus included in the \( I_{dsat} \) model (the solid line in the figure).

Fig. 2 illustrates that the new model is accurate because all the effects, i.e., mobility degradation, LDD channel series resistance, and \( V_t \) roll-off, have been included in the model. Otherwise, as shown by the dashed and dotted lines, they are not fitting the measurement data. Fig. 3 shows that the new semi-empirical model fits measurement data for three different technologies.

To get an insight for future technology's driving capability trend, simulated \( I_{dsat} \) versus \( L_{eff} \) for fixed \( V_t \) and \( R_s \) with different \( T_{ox} \) and power supply voltage are plotted in Fig. 4. In this plot, \( V_t \) is fixed at 0.7 V and 0.5 V, respectively. This is generally true for mature technologies where \( V_t \) does not vary much for a relatively large range of \( L_{eff}. \) Two typical values of \( R_s \) as mentioned earlier, 400 \( \Omega \cdot \mu \text{m} \) and 800 \( \Omega \cdot \mu \text{m} \), have been chosen for this plot. For each chosen technology, i.e., \( T_{ox} \) and \( V_{dd}, I_{dsat} \) for three out of four different \( V_t \) (0.5 V and 0.7 V) and \( R_s \) (400 \( \Omega \cdot \mu \text{m} \) and 800 \( \Omega \cdot \mu \text{m} \) combinations are plotted. To be more practical, for larger \( V_{dd} \) and \( T_{ox} \), larger \( V_t = 0.7 \text{ V and } R_s = 800 \text{ } \Omega \cdot \mu \text{m} \) are emphasized. For thinner \( T_{ox} \) and smaller \( V_{dd} \), smaller \( V_t = 0.5 \text{ V and } R_s = 400 \text{ } \Omega \cdot \mu \text{m} \) are stressed because better technologies to reduce source and drain series resistances for future generations are reasonably assumed. Because the physics and effects modeled in this paper are believed to continue to dominate to lower \( L_{eff} \) which is not compared with real data, the plot shows \( I_{dsat} \) down to \( L_{eff} = 0.2 \mu \text{m}. \) For even smaller \( L_{eff}, \) other effects such as velocity overshoot may start showing up and the accuracy by the model presented here needs to be modified accordingly for that regime. Fig. 4 illustrates that due to mobility degradation and power supply scale down, future peak \( I_{dsat} \) will usually remain at the range of 0.35–0.6 mA/\( \mu \text{m}. \)

III. CONCLUSIONS

It has been shown that with the new empirical mobility expression that is solely dependent on \( V_{gs}, V_t, \) and \( T_{ox}, \) the

\[
I_{dsat} = \frac{V_t + 2(V_{gs} - V_t) R_s W \nu_{sat} C_{ox} - \sqrt{V_t^2 + 4(V_{gs} - V_t) E_{sat} L_{eff} W \nu_{sat} C_{ox}}}{2(R_s + W \nu_{sat} C_{ox} R_s^2)}
\]

(5)
corresponding new $I_{\text{dsat}}$ model considering the effects of mobility degradation with rising vertical field, source and drain series resistance, velocity saturation, and $V_t$ roll-off shows good agreement with the measurement data for several different technologies. Future trends for device scaling and low-power applications can be predicted correctly by this new model. The new model shows that the maximum $I_{\text{dsat}}$ for future MOSFET's may remain in the range of 0.35–0.6 mA/μm. Even though the discussion so far has been limited to the n-MOSFET, similar work can be done for p-MOSFET as well. The results for the p-MOSFET $I_{\text{dsat}}$ modeling will be presented in a separate paper.

REFERENCES
