Sub 50-nm FinFET: PMOS

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Abstract

High performance PMOSFETs with gate length as short as 18-nm are reported. A self-aligned double-gate MOSFET structure (FinFET) is used to suppress the short channel effect. 45 nm gate-length PMOS FinFET has an I_{dsat} of 410 μA/μm (or 820 μA/μm depending on the definition of the width of a double-gate device) at Vd = Vg = 1.2 V and Tox = 2.5 nm. The quasi-planar nature of this variant of the double-gate MOSFETs makes device fabrication relatively easy using the conventional planar MOSFET process technologies. Simulation shows possible scaling to 10–nm gate length.

Introduction

The double-gate MOSFET is considered the most attractive device to succeed the planar CMOS transistors when the latter can not be scaled further [1]. The FinFET, a recently reported novel double-gate structure, consists of a vertical Si fin controlled by self-aligned double-gate [2] . In spite of its double-gate structure, the FinFET is close to its root, the conventional MOSFET in layout and fabrication. The features of this structure include (1) an ultra-thin Si fin for suppression of short-channel effects; (2) two gates which are self-aligned to each other and to the source/drain (S/D) regions; (3) raised (poly-Si) S/D to reduce parasitic resistance; (4) a short (50 nm) Si fin for quasi-planar topography; and (5) gate-last process compatible with low-T, high-k gate dielectrics. N-channel FinFETs showed good short-channel performance down to 17 nm gate length [3]. In this paper, we report P-channel FinFET results, demonstrating the promise of the FinFET structure as a future CMOS technology.

Device Fabrication

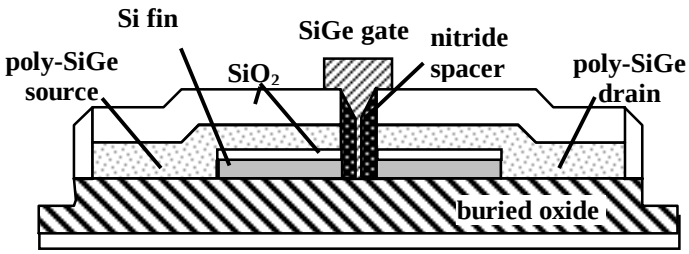

Figure 1: Schematic drawing of FinFET

Fig. 1 shows an exploded view of the FinFET device. The following process sequence was used to fabricate the device. 100 nm SOI film over buried oxide was thinned to 50 nm by thermal oxidation. Ion implantation established a body doping concentration of 10^{16} cm^{-3}. Then LTO was deposited over the Si film as a hard mask material. Using 100 keV e-beam lithography and resist ashing in O_2 plasma, narrow Si fins were patterned and etched. 100 nm in-situ boron-doped SiGe and 300 nm LTO hard mask were deposited over the fin. SiGe is used because the resistivity of heavily doped p-type poly-$Si_{1-x}Ge_x$ is much lower than that of comparably doped poly-Si [4]. The SiGe provides good electrical contact at the side surfaces of the Si fin. The LTO and SiGe films were etched to delineate and separate the raised source and drain regions. **Fig. 2** shows the S/D with a gap in-between. Visible in the gap is the Si fin with the oxide hard mask. 100 nm nitride was then deposited and etched to form spacers on the side-walls of the S/D. By sufficient overetching, nitride was removed from the side-walls of the fin. **Fig. 3** shows a <20 nm gap between the S/D spacers. (The fin is difficult to see at the center of the photo.) The width of this spacer gap at the sides (not the top of the fin/hardmask) determines the gate length. 15 nm of sacrificial oxide was grown and wet etched to remove the damage created by the dry-etching processes from the side surfaces of the fin. This step further reduces the fin thickness. The final thickness of the fins ranged from 15 nm to 30 nm. 2.5nm gate oxide was grown on the side surfaces of the fin at 750°C. This "high

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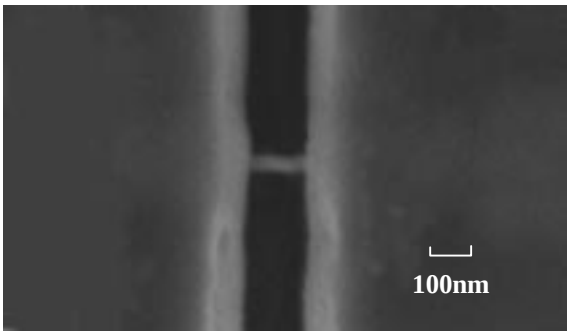


Figure 2: SEM top view after source/drain etch. A thin fin is visible in the gap between source & drain and will be further thinned by sacrificial oxidation.

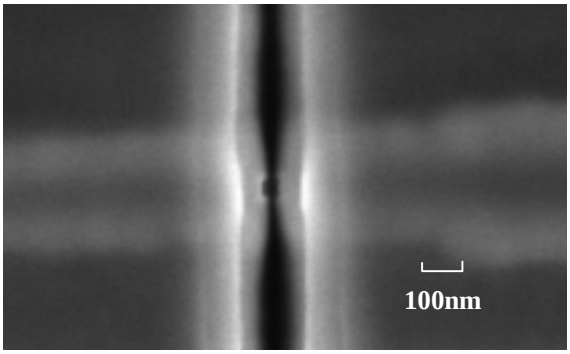


Figure 3: SEM top view after nitride spacer etch. Si fin is at the center of the photo. The gap between spacers at the sides of the fin is less than 20nm. This gap defines the gate length.

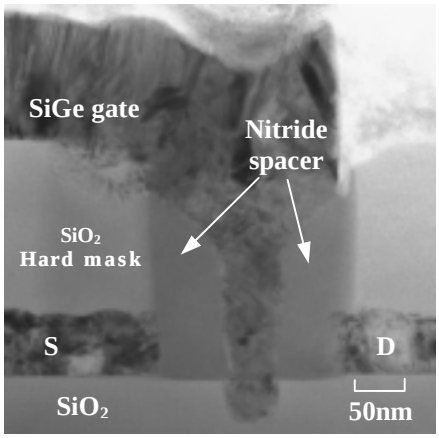


Figure 4: Cross-sectional TEM picture: gate is defined by the gap between nitride spacers.

temperature" step combined with an additional annealing step, drove boron from the SiGe raised S/D regions into the fin underneath the nitride spacers to form P+ S/D extensions. After depositing 200 nm of in-situ-doped SiGe (60% Ge, with a workfunction of 4.75 eV) as the gate material, the gate electrode was patterned and etched. The cross-sectional TEM picture in **Fig. 4** shows the excellent vertical gate and spacer profile. The gate length of the TEM test structure, which is around 50 nm as seen in **Fig. 4**, is drawn longer than that of the real devices. Finally, windows were etched through the oxide hardmask to allow for direct probing of the poly-SiGe source and drain pads. No metallization was used in this experiment to allow for the option of further thermal drive-in annealing.

Device Performance

Fig. 5 shows the I-V characteristics of a 18-nm gate length device with a 15 nm-thick Si fin body. I_{dsat} is 288 µA/µm at Vd = Vg = 1.2 V. **Fig. 6** shows the I-V characteristics of a 45-nm gate length device with a 40 nm-thick Si body. I_{dsat} is 410 µA/µm at Vd = Vg = 1.2 V. In this paper, we count the device width as twice the fin height. A more aggressive definition of the width of a double-gate FET would have doubled the current density to 820 µA/µm .

Vt roll-off characteristics are shown in **Fig. 7.** Vt is defined as the gate voltage when Ids = 50 nA/µm for Vd = 0.05 V. **Fig. 8** shows the subthreshold swing dependence on gate length. Good short-channel characteristics are observed for the double-gate FinFET structure. **Fig. 9** shows the

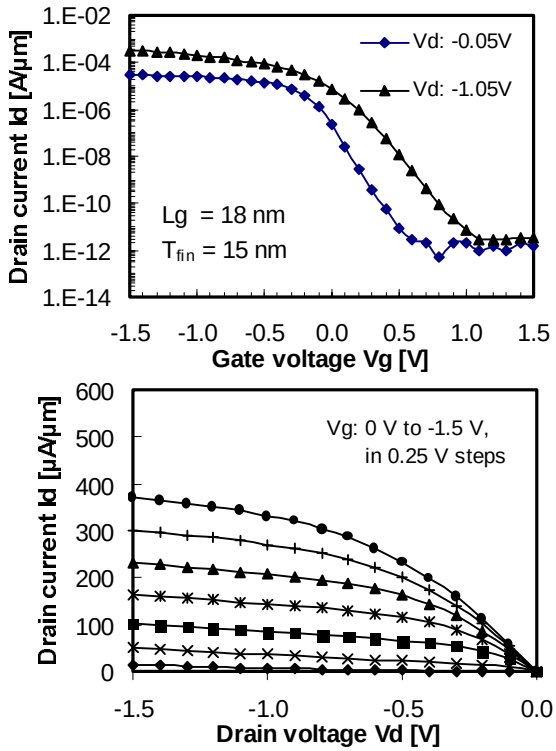
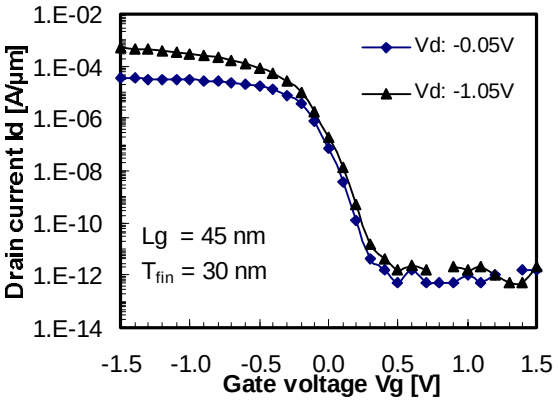


Figure 5: IV characteristics of PMOS FinFET with 18-nm gate length and 15-nm Si fin body.



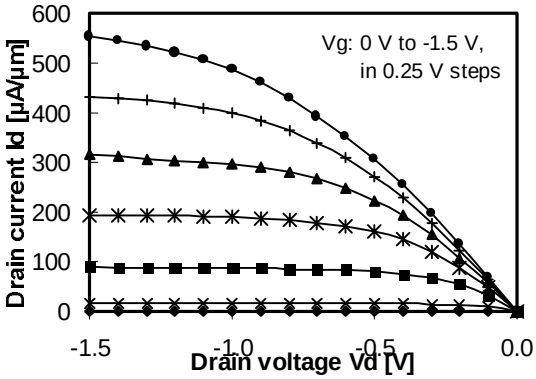


Figure 6: IV characteristics for 45-nm gate length and 30-nm thick Si body PMOS device

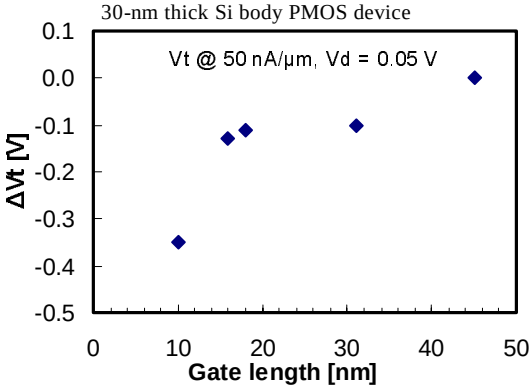


Figure 7: Vt roll-off characteristics

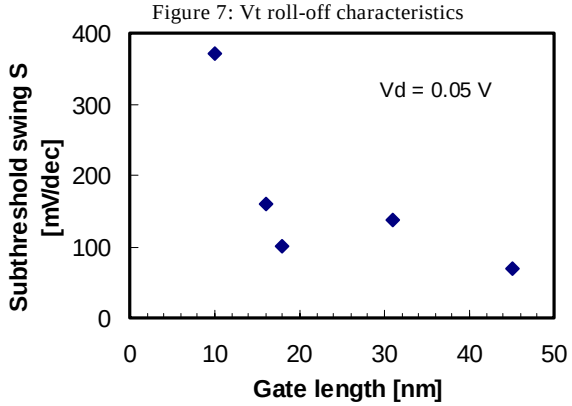


Figure 8: Subthreshold swing vs. gate length.

subthreshold swing dependence on the Si-fin width. We can see that the subthreshold swing worsens with increasing fin

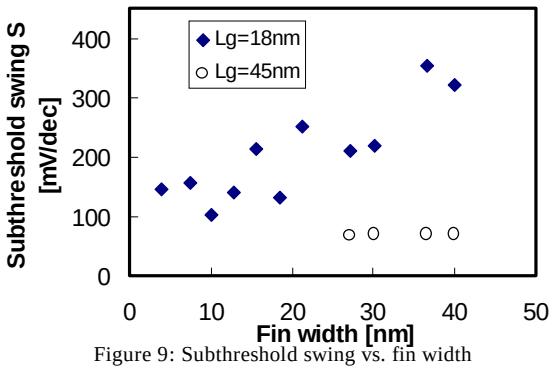


Figure 9: Subthreshold swing vs. fin width

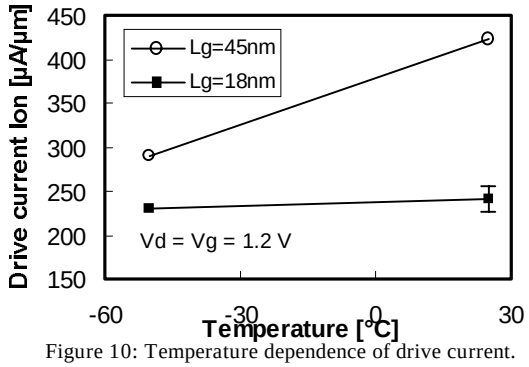


Figure 10: Temperature dependence of drive current.

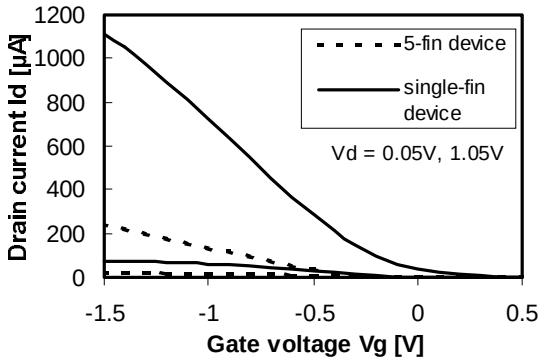


Figure 11: FinFET width can be adjusted quasi-continuously by the increment of a sigle fin (50-nm height)

width, which is the body thickness. It appears that fin width can be as large as 70% of the gate length without degrading the swing with the S/D design used in this study.

Fig. 10 shows the temperature dependence of the drive current. It is observed that the drive current is reduced as the temperature goes down. This is opposite to the usual MOSFET behavior. It is tempting to take this as an indication of ballistic transport. However the gate-length dependence doe not support this interpretation. Further study is needed to elucidate the temperature effect.

FinFET is designed to use multiple-fins to achieve larger channel widths. The S/D pads straightforwardly connect the

fins in parallel. Multi-fin devices were fabricated and results are presented in **Fig. 11**. The 5-fin device conducts 5 times more current than the single fin device. Although the channel width can be varied only in increments of 2× the fin height, this is not a serious design constraint because the increment is small (50 nm fin height) in the current process.

The experimental data obtained in this experiment closely matches 2-D device simulations that assume simple Gaussian doping profiles and a uniformly doped channel region. Drift-diffusion simulation underestimates the current by 15% for the 45-nm device. The energy balance model was found to give excellent agreement with experimental data. **Fig. 12** shows the results for both the on-state and off-state currents. Employing the same simulation model and source-drain diffusion profiles which match experimental results of the 45-nm and 18-nm devices, the performance of a 10-nm FinFET was simulated (**Fig. 13**). By aggressively scaling the gate oxide thickness (1.2 nm) and the silicon fin width (7 nm), a drive current of 347 μA/μm, or 694 μA/μm, depending on the definition of device width, can be achieved while still maintaining low leakage (2.3, or 4.6 nA/um) and minimal short-channel effects. This is due to the excellent short-channel behavior of the double-gate MOSFET structure.

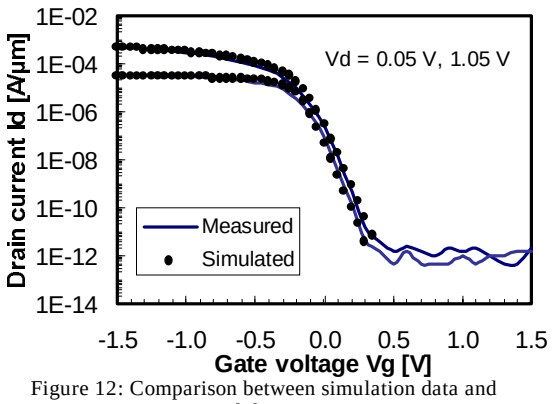


Figure 12: Comparison between simulation data and experimental data.

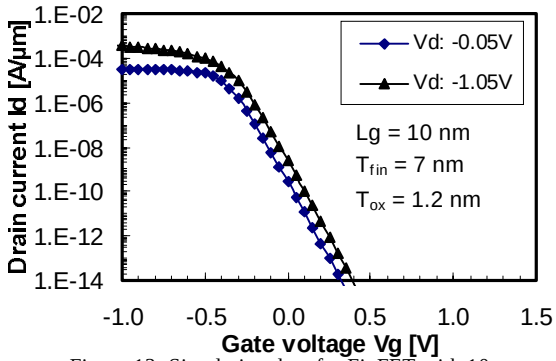


Figure 13: Simulation data for FinFET with 10-nm gate length. I_{dsat} = 347 (or 694) μA/μm for Vg = Vd = 1.2 V, and I_{off} = 2.3 (or 4.6) nA/μm.

Conclusion

Sub 50-nm p-channel FinFETs were successfully fabricated. These devices exhibited good performance characteristics down to 18-nm. The formation of an ultra-thin (< 0.7Lg) Si body is critical for suppressing short-channel effects. Low-resistance contacts to the ultra-thin Si fin were formed using doped poly-SiGe films for raised S/D contacts, so that high drive currents (410 μA/μm, or 820 μA/μm depending on width definition) were attained at Vd = Vg = 1.2 V. This structure is fabricated by forming the S/D before the gate, a technique that may be needed for future high-k dielectric and metal gate technologies that can not tolerate the high temperature required for S/D formation. The FinFET is an attractive successor to the single-gate MOSFET.

Acknowledgement

The authors would like to thank the UC Berkeley Microlab Staff for their support in device fabrication. This work made use of the National Nanofabrication Users Network facilities funded by the National Science Foundation under award number ECS-9731294. This research is sponsored by DARPA AME program under Contract N66001-97-1-8910.

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