CIRCUIT AGING SIMULATOR (CAS)

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ABSTRACT

A Circuit Aging Simulator (CAS) has been developed as part of the BSIM (Berkeley Short-channel Igfet Model) family to predict the effects of hot-electron degradation on MOS circuit behavior. Using the well-known SPICE2 or SPICE3 circuit simulator in a UNIX environment, CAS simulates circuit behavior at a user-specified future time point using fresh and DC pre-stressed BSIM parameter process files. CAS is configured in a pre- and post-processor configuration so that no modifications to the SPICE code is necessary. Iterative simulation to take into account ongoing degradation can also be done through an accompanying UNIX shell script program.

I. INTRODUCTION

Hot-electron degradation is becoming an increasingly worrisome issue as device dimensions continue to shrink while the power supply voltage remains constant for compatibility. The high electric fields within these smaller devices accelerate the degradation process, causing device characteristics to change. Presently, research and testing have concentrated on device-level degradation parameters such as the threshold voltage shift ΔV_{th}, drain current reduction $\Delta I_{ds}/I_{ds0}$, and transconductance degradation $\Delta g_m/g_{m0}$, to quantify the amount of device degradation that has occurred. Calculating device lifetime based on these parameters can provide important information on the amount of degradation occurring in each device of the circuit and identify "hot spots" that need to be alleviated. The Substrate Current And Lifetime Evaluator (SCALE) processor [1][2] was developed for this purpose as well as to produce transient substrate current waveforms. Thus, in addition to lifetime calculations, a check, for instance, can be made as to whether the substrate bias generator can handle the total substrate current generated by the circuit.

It remains unclear, however, on how to relate the device-level degradation parameters directly to circuit output behavior and performance. Aur et al [3] have already demonstrated the fact that not all devices will affect the circuit output equally. They have shown that each device may have different performance sensitivities towards the output, and that this relationship may also change with the power supply voltage. These sensitivities will also undoubtably change as node capacitances and relative device dimensions vary.

The Circuit Aging Simulator (CAS) has thus been developed as an addition to the Berkeley Short-channel Igfet Model (BSIM) family to (1) predict the amount of degradation each transistor suffers while operating in a circuit environment for a user-definable length of time, and (2) to directly simulate the entire circuit using degraded device parameters obtained from the information found in (1). CAS is a superset of SCALE in that transient substrate current waveforms and device lifetimes can still be calculated. In addition to the three degradation parameters needed by SCALE, CAS uses separate BSIM parameter sets extracted from successively DC-stressed devices to calculate the degraded parameter set needed for aged circuit simulation. As an added feature, a UNIX shell script has been developed for user-friendliness and to make possible automated iterative simulations to take into account on-going circuit degradation.

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II. MODEL IMPLEMENTATION

The two models incorporated in CAS in addition to the BSIM drain and substrate current models are the device degradation and lifetime model, and device aging model. The degradation model is identical to that incorporated in SCALE [1][2] with the exception that bias dependencies of two of the degradation parameters (m and H) with respect to gate-to-drain voltage V_{gd} have been implemented. The device aging model adds the capability to calculate new aged parameter sets from parameters extracted from the DC-stressed devices and is discussed below.

Circuit Aging Model

To calculate new aged parameters from pre-stressed devices, we introduce a quantity *Age* which provides the means to compare the amount of degradation suffered by the device in the circuit to that of the pre-stressed devices. This quantity is directly related to the amount of degradation that takes place. Since we know that the threshold voltage shift ΔV_{th}, and the drain current and transconductance degradation ($\Delta I_{ds}/I_{ds0}$ and $\Delta g_m/g_{m0}$ respectively) do have a direct relationship to the amount of degradation that has occurred, we can, from Refs. [1][2][4], describe this degradation by the form

$$Degradation \;\alpha\; At^n = \left[\frac{I_{ds}}{WH}\left[\frac{I_{bs}}{I_{ds}}\right]^m\right]^n t^n$$

Here we have used $H = B/Degradation_f$ rather than B used in [1][2] to eliminate the dependence of the degradation parameters on the criteria chosen to define device lifetime ($t = \tau$ = lifetime when $Degradation = Degradation_f$). We can now introduce an *Age* variable that is directly related to this degradation as well as being based on time :

$$Degradation \;\alpha\; (\,Age\,)^n$$

$$Age = \frac{I_{ds}}{WH}\left[\frac{I_{bs}}{I_{ds}}\right]^m t \qquad (1)$$

During circuit simulation, the *Age* is calculated for each device at each timestep, then summed to obtain the total *Age* of the SPICE analysis.

To calculate the *Age* of each device at a user-specified time T_{age}, it is assumed that circuit behavior is periodic with the period equal to the length T of the SPICE analysis. The age that each device would then have at T_{age} becomes

$$Age\,(T_{age}) = Age\,(T)\left[\frac{T_{age}}{T}\right]$$

The list of ages for every device in the circuit is stored in an external

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file called "agetable" to be used for the next step, the creation of aged process files.

Now with the *Age* of each device in the circuit computed, and the *Age* of each of the pre-stressed device parameter sets calculated beforehand, the actual aged parameters for the circuit device are calculated by interpolating each parameter from the pre-stressed device parameters using the log(*Age*) variable as the abscissa:

$$P_{age} = \left[\frac{\log(Age) - \log(Age_i)}{\log(Age_{i+1}) - \log(Age_i)} \right] (P_{i+1} - P_i) + P_i$$

where i and $i+1$ represent two successive times when parameter extraction is done. Figs. 1 and 2 show some of the BSIM parameters varying with respect to time for the DC pre-stressed device (The *Age* would equal the time multiplied by a constant in this case). The circuit device would normally fall within two of the extracted points (such as the point labeled "A" on Figs. 1 and 2). Fig. 3 shows the measured and simulated drain current using fresh and stressed process files for V_{gs} = 5 V.

In summary, the following is done for circuit aging simulation:

(1) The user extracts BSIM parameters from a fresh device, followed by successive extractions of the same device after it has been DC-stressed for different lengths of time.

(2) The user calculates the *Age* of each of the extracted process files by using equation (1).

(3) CAS simulates the desired circuit and calculates the *Age* that each device in the circuit would have if the SPICE analysis is repeated up to the user-specified future time point.

(4) CAS compares the *Age* of each device in the circuit with that of the stressed BSIM process files of step (2), and calculates the new aged process files by interpolation.

(5) The aged circuit can now be simulated using SPICE with these aged parameters.

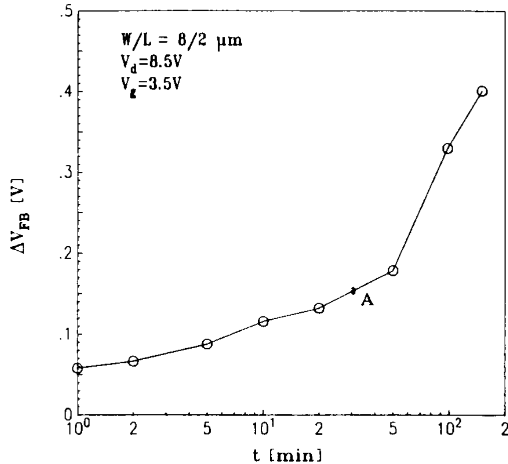

Fig. 1

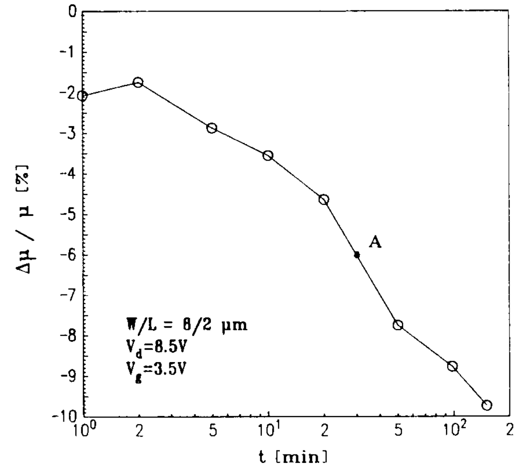

Fig. 2

Figs. 1, 2 Examples of the BSIM parameter degradation by hot-carrier stress. Although here we use stress time as the horizontal axis, $[I_{sub}/I_{ds}]^m (I_{ds}/W)\Delta t$ is used as the 'age' parameter in simulation. Fig. 1 : flat band voltage, V_{FB}, Fig. 2 : linear region mobility, μ.

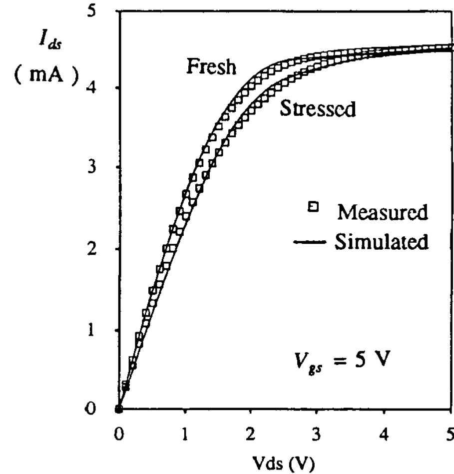

Fig. 3 A comparison of the measured and simulated drain current versus V_{ds} at V_{gs} = 5 V for a fresh and a stressed device.

III. SYSTEM CONFIGURATION

CAS is configured in a pre- and post-processor configuration to SPICE, as shown in Fig. 4. Because of this fact, no modifications are necessary to the SPICE code itself. Presently, CAS supports SPICE3 and the special version of SPICE2G.6 containing the BSIM model.

As mentioned previously, a menu-driven UNIX shell script program is also available to further simplify the use of CAS. More importantly, an option is available to divide the total age time into equal intervals, and then to calculate a set of degraded parameters for each interval to be used for the next time interval. In this way, on-going device degradation can be taken into account.

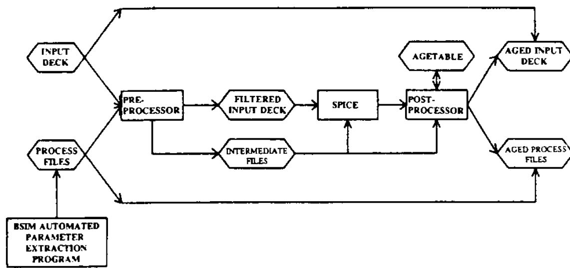

Fig. 4 Schematic configuration of the system. The BSIM(Berkeley Short-Channel IGFET Model) Automated Parameter Extraction Program extracts the model parameters for the drain current and substrate current.

IV. EXPERIMENTAL AND SIMULATION RESULTS

Some experimental and simulated results of both analog and digital circuits are presented in this section.

Analog Circuit Example : NMOS Operational Amplifier

A simple NMOS operational amplifier, having the same configuration as in Ref. [5], is studied as an analog circuit example (Fig. 5). Minimum channel length is 2 μm. The circuit was stressed at an inverting input of 5V, a non-inverting input of 0V, and a supply voltage of 10V. Table 1 shows the agetable which gives the *Age* of some of the individual devices in the circuit. By inspection, transistors M13 and M21 suffer significant degradation according to the simulated results. Since both M13 and M21 make up the output stage of the circuit, the degradation of these devices has little effect on the gain of the amplifier; the input offset voltage, however, is affected. Fig. 6 shows the time evolution of both experimental and simulated input offset voltage. The trend obtained by simulation agrees well with the experimental results, although the amount of change is somewhat different. The error is believed to be due to inaccuracy in m.

Digital Circuit Example : 16-Stage CMOS Inverter Chain

A simulated digital circuit example, that of a 16-stage CMOS inverter chain (Fig. 7), is shown in Figs. 8 - 10. The circuit was run at V_{dd} = 5 V, with a 100 MHz clock signal as input for a time duration of 100 years. A decrease in propagation delay degradation is seen if the aspect ratio is increased (Fig. 8). When circuit loading is varied instead, an interesting non-monotonic effect can be seen (Fig. 9). Fig. 10 clearly demonstrates that the monotonic device-level degradation behavior can be misleading in predicting circuit degradation.

Discussion

From other extensive simulations using CAS, it has been found that certain digital circuits based on inverter-like blocks can tolerate a large amount of device degradation without suffering excessive circuit degradation. This can be seen by comparing Figs. 9 and 10 and noting that a 20% change in drain current or transconductance degradation, or nearly a 100 mV change in the threshold voltage, generates only 1.5% to 2.5% degradation in circuit performance. One reason that such a discrepancy is seen is that $\Delta I_{ds}/I_{ds0}$ is typically taken at V_{gs} = 5 V and V_{ds} = 50 mV, whereas the degradation that has the most effect to circuit operation is $\Delta I_{ds}/I_{ds0}$ at $V_{ds} \approx V_{dd}/2$ (Fig. 3). The effect of the NMOS degradation is further reduced by the fact that the PMOS device, which degrades little, is responsible for half of the delay in a properly ratioed circuit. Overall, even if $\Delta I_{ds}/I_{ds0}$ was measured at $V_{ds} \approx V_{ds}/2$, only a third or a fourth of this degradation is seen at the output of the circuit. Finally, because substrate current generation occurs only during the V_{gs} - V_{ds} overlap of the CMOS logic gate, degradation is directly related to the clock rate rather than the duty cycle.

There are cases, however, that CAS underestimates the amount of degradation that takes place for a few circuit types in which the NMOS device experiences a high-to-low V_{gs} transient during high V_{ds} [1][2], such as when a wide PMOS-device inverter experiences a slow input voltage fall. Such enhanced degradation models are planned to be included in future CAS versions.

Although digital circuits seem to be more robust than previously thought, it is anticipated that analog circuits may be more susceptible to hot-carrier degradation. Because of their need of symmetry between devices, a slight mismatch caused by degradation can cause noticeable performance changes, such as the offset voltage drift shown in Fig. 6.

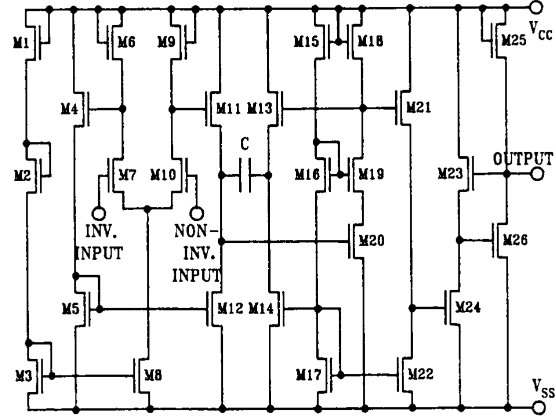

Fig. 5 Circuit configuration of the NMOS operational amplifier used here. Minimum channel length is 2 μm and oxide thickness is 20nm.

Device Name	Process Name	Age	Vds(V)	Vgs(V)
M21	PC2 nm1 du1	1.003760e+00	9.989	0.335
M13	PC2 nm1 du1	8.384320e-01	9.978	0.324
M23	PC1 nm4 du1	5.207166e-04	8.457	0.955
M4	PC1 nm5 du1	1.177822e-09	9.062	6.688
M11	PC1 nm5 du1	1.061775e-09	8.517	6.793
M8	PC1 nm4 du1	2.912096e-11	3.849	1.090
M7	PC2 nm1 du1	1.394939e-11	3.777	1.151
M25	PC1 nm5 du1	4.040922e-14	7.502	7.502
M26	PC1 nm4 du1	9.684229e-25	2.498	1.543

Table 1 An example of the "agetable" after 10 minutes' stress.

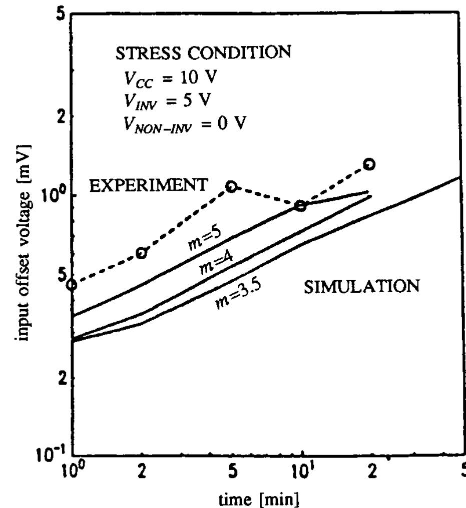

Fig. 6 Time evolution of the equivalent input offset voltage.

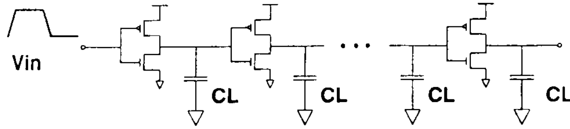

Fig. 7 Sixteen-stage CMOS inverter stage simulated by CAS. W_n = 20 μm, $L_{eff_n} = L_{eff_p}$ = 1.0 μm. Capacitive loading C_L and PMOS device width W_p were varied to investigate their effects on aging.

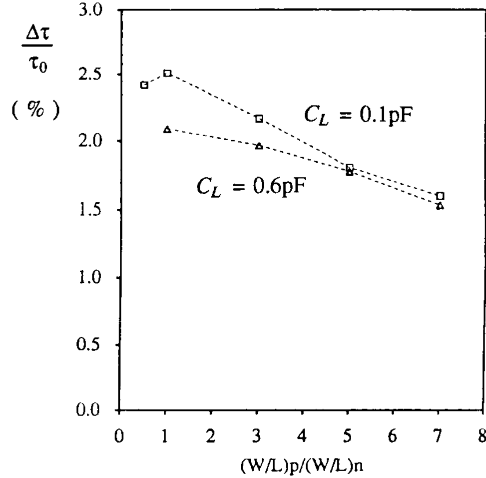

Fig. 8 Propagation delay degradation versus aspect ratio (W/L)p/(W/L)n after running the inverter chain for 100 years at V_{dd} = 5 V. C_L = 0.1 pF and 0.6 pF.

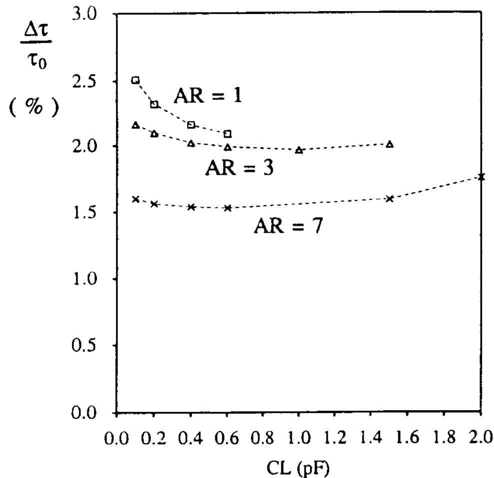

Fig. 9 Propagation delay degradation versus capacitive loading after running the inverter chain for 100 years at V_{dd} = 5 V. Aspect ratio = AR = 1,3 and 7. Note the apparent decrease, then increase in the frequency degradation as the loading is increased.

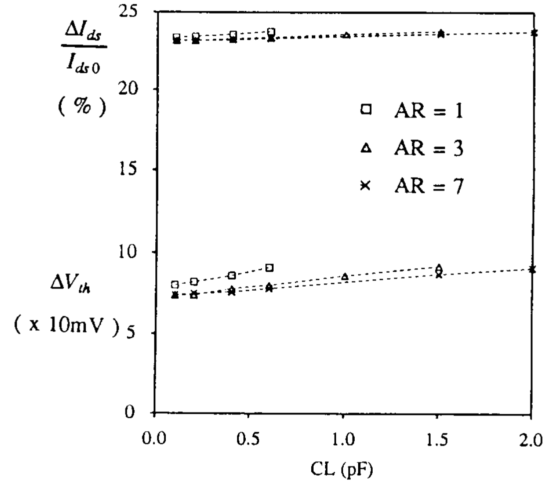

Fig. 10 The device-level degradation parameters $\frac{\Delta I_{ds}}{I_{ds0}}$ and ΔV_{th} versus C_L for AR = 1,3 and 7 after 100 years. Note the monotonic increase in device-level degradation in contrast to the propagation delay degradation in Fig. 9.

V. CONCLUSION

CAS has been developed to predict the time evolution of MOS circuit performance degradation caused by hot carriers. CAS is fully capable of simulating circuit aging for either static or dynamic circuit operation. Circuit designers can simulate the hot-carrier degradation of their circuits by using CAS and can study and improve the reliability of their circuits accordingly.

Acknowledgements

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References

[1] M.M. Kuo, K. Seki, P.M. Lee, J.Y. Choi, P.K. Ko, and C. Hu, "Quasi-static simulation of hot-electron-induced MOSFET degradation under (ac) pulse stress," *International Electron Devices Meeting Technical Digest*, pp. 47-50, December 1987.

[2] M.M. Kuo, K. Seki, P.M. Lee, J.Y. Choi, P.K. Ko, and C. Hu, "Simulation of MOSFET lifetime under ac hot-electron stress," *IEEE Trans. on Electron Devices*, Vol. 35, No. 7, pp. 1004-1011, July 1988.

[3] S. Aur, D.E. Hocevar, and P. Yang, "Circuit hot electron effect simulation," *International Electron Devices Meeting Technical Digest*, pp. 498-501, December 1987.

[4] C. Hu, S.C. Tam, F.-C. Hsu, P.K. Ko, T.Y. Chan, and K.W. Terrill, "Hot-electron-induced MOSFET degradation - Model, monitor, and improvement," *IEEE Trans. Electron Devices*, Vol. ED-32, No. 2, pp. 375-385, February 1985.

[5] Y.P. Tsividis, P.R. Gray, "An integrated NMOS operational amplifier with internal compensation," *IEEE J. Solid-State Circuits*, Vol. SC-11, p.748-754, December 1976.