

The effect of channel hot carrier stressing on gate oxide integrity in MOSFET

I. C. Chen¹, J. Y. Choi, T. Y. Chan, T. C. Ong, and C. Hu

Department of Electrical Engineering and Computer Sciences
University of California, Berkeley
Berkeley, CA 94720

Abstract

The correlation between channel hot carrier stressing and gate oxide integrity is studied. It is found that channel hot carriers have no detectable effect on gate oxide integrity even when other parameters (e.g. ΔV_T and ΔI_D) has become intolerably degraded. In the extreme cases of stressing at $V_G \approx V_T$ with measurable hole injection current, however, the oxide charge-to-breakdown decreases linearly with the amount of hole fluence injected during the channel hot hole stressing. This may limit the endurance of a non-volatile memory using hot holes for erasing. This can also explain the gate-to-drain breakdown of a device biased in the snap-back region, since snap-back at low gate voltage is favorable for hole injection. Snap-back induced oxide breakdown could be an ESD failure mechanism.

Introduction

Thin gate oxide wearout is one of the major reliability concerns for MOS integrated circuits. The mechanism of oxide time-dependent-breakdown has been attributed to charge trapping [1,2] or interface state generation [3] in the oxide. Recently, we have demonstrated a close correlation between oxide breakdown and hole trapping with holes generated within the oxide or in the anode electrode by energetic electrons injected via Fowler-Nordheim (F-N) tunneling [4,5]. One wonders whether externally injected hot-carriers (e.g. channel hot-carriers) into the oxide would have a similar detrimental effect on oxide integrity. This question is of particular interest

¹presently with Semiconductor Process and Design Center, Texas Instruments, Dallas TX 75265

to some recent proposals of using hot-holes to erase the stored electrons in a nonvolatile memory [6,7] and also to some applications, e.g. ESD protection device, where snap-back occurs with gate grounded. If the answer is yes, one further questions the relative importance of oxide wearout vs. MOSFET characteristics degradation (e.g. threshold voltage shift) due to hot carrier stressing. These questions are the motivations of the present work.

Channel hot carrier, rather than substrate hot carrier, stressing is employed as the carrier injection scheme because of the practical interest mentioned above as well as the versatility of injecting either electrons or holes into the oxide [8,9], which could also provide some independent evidence regarding the mechanism of oxide breakdown.

Experiment

Silicon gate n-channel MOSFET's fabricated in three different laboratories were used in this study. The starting materials for the three kinds of devices are boron-doped (100) oriented Si wafers with dopant concentration of 8×10^{15} , $7 \times 10^{16} \text{ cm}^{-3}$ and 2×10^{16} respectively. The gate oxides for the three wafers were grown in dry oxygen at around 950°C to the thicknesses of 200, 90, and 230 Å, respectively. In-situ doped poly-silicon was then deposited at 650°C and annealed at 900°C for 20 min in N_2 . LDD structure was fabricated in the third group of devices used where the N^- implant dosage is around $2 \times 10^{13} \text{ cm}^{-2}$. After source/drain implantation (As, 5×10^{15} , 120 keV), the wafers were annealed in N_2 at 950°C for an hour. The post metalization sintering was performed in forming gas at 425°C for 20 min.

Channel hot carrier (CHC) stressing was performed at various gate voltage, V_G , under fixed drain voltage, V_D , as shown in Fig.1a. Threshold voltage shift, ΔV_T , as well as the percentage degradation of drain current, $\Delta I_D/I_D$, were recorded after the CHC stressing for 1 or 2 hours, where V_T is defined as the V_G at which I_D is equal to W/L (channel width/length) in μA and $\Delta I_D/I_D$ was measured at $V_G = 5$ V with $V_D = 50$ mV for both measurements. After these measurements, the source and drain of the transistor were grounded to the substrate and a constant F-N tunneling current ($J_G = -0.1 A/cm^2$) was applied to the gate, as shown in Fig.1b, until the destructive breakdown of the gate oxide occurs. Charge-to-breakdown, Q_{BD} defined as $J_G \cdot t_{BD}$ where t_{BD} is the time-to-breakdown of the oxide, was also recorded as an indication of the oxide integrity after the channel hot-carrier stressing. In this paper all J_G and Q_{BD} are calculated by dividing current and

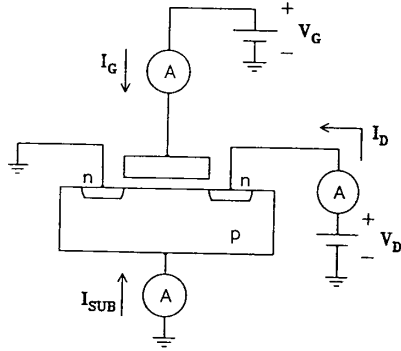


Figure 1a The connection diagram for channel hot carrier (CHC) stressing. Threshold voltage shift, ΔV_T , and current degradation, $\Delta I_D/I_D$, are recorded after the stressing.

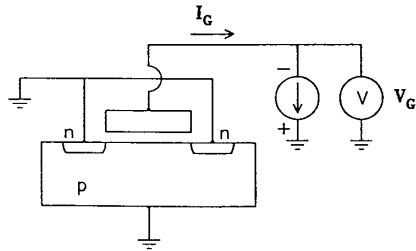


Figure 1b The connection diagram for oxide integrity test. The charge-to-breakdown, Q_{BD} , of the gate oxide under a constant current stressing is recorded as an indication of the oxide integrity after the CHC stressing.

charge by the area $W \cdot L$, as if the current were uniformly distributed over the gate area. This is done for simplicity and does not affect the basic conclusion of the study. In the case of snap-back stressing at low gate voltage, a ramp-voltage I-V measurement follows the stressing, and the breakdown current in the F-N I-V curve is used as an relative indication of oxide integrity.

Channel Hot Carrier stressing without significant hole current

Fig.2a shows the well-known bell-shaped substrate current, I_{SUB} , and gate current, I_G , of a 200 Å gate oxide transistor with $W/L = 20/2$ (μm) measured at $V_D = 8$ V. The gate current peaking at $V_G \simeq V_D$ is due to channel hot-electron injection into the oxide [8,9]. Fig.2b and Fig.2c show the ΔV_T and $\Delta I_D/I_D$ for such devices stressed at the

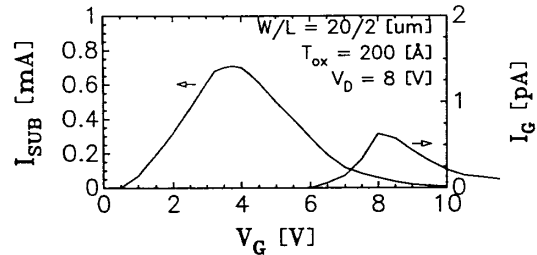


Figure 2a The well-known bell-shaped I_{SUB} and I_G of an n-channel MOSFET measured as a function of V_G with V_D fixed at 8 V. The oxide thickness and W/L of the device are 200 Å and 20/2 μm respectively. The I_G peaked at $V_G \simeq V_D$ is due to channel hot-electron injection, while the hot-hole injection current is below the detection limit.

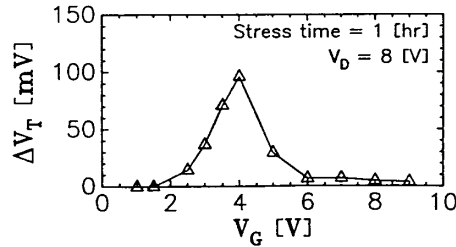


Figure 2b Threshold voltage shift, ΔV_T , vs. V_G for devices stressed under the bias condition shown in Fig.2a for 1 hour. The peak value of ΔV_T is around 100 mV, which is much larger than the usual 10 mV lifetime definition.

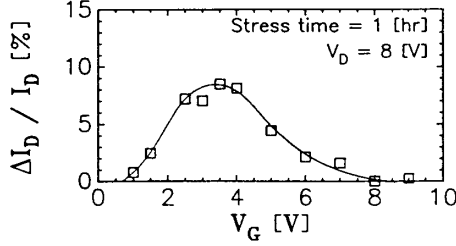


Figure 2c Drain current degradation, $\Delta I_D / I_D$, as a function of V_G after the same stressing. The peak $\Delta I_D / I_D$ value, 8.5 %, is also much larger than the commonly used 3 % lifetime definition.

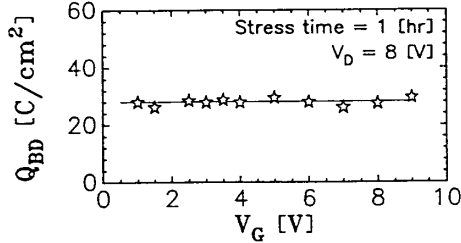


Figure 2d Charge-to-breakdown, Q_{BD} , under a constant gate current ($J_G = -0.1 \text{ A/cm}^2$) stressing for devices having experienced the channel hot carrier stressing shown in Fig.2a to Fig.2c. The nearly constant Q_{BD} 's suggest oxide integrity is not influenced by the channel hot carrier stressing shown in Fig.2a.

bias conditions shown in Fig.2a for an hour. The bell-shaped curves shown in the figures resembles that of the I_{SUB} as expected, supporting the notion that I_{SUB} is a good indicator of device degradation rate [10]. Because of the severe biasing condition, V_D is less than the minimum snap-back voltage by only 0.5 V, the peak values of ΔV_T and $\Delta I_D / I_D$ shown in Fig.2b & c, 100 mV and 8.5 % respectively, are beyond the commonly used MOSFET lifetime definition of $\Delta V_T = 10 \text{ mV}$ and $\Delta I_D / I_D = 3 \%$. However, when these severely degraded MOSFET's were subject to a constant gate current stressing ($J_G = -0.1 \text{ A/cm}^2$) with grounded source/drain, the Q_{BD} values were unchanged as shown in Fig.2d, independent of the CHC stressing history. This suggests that although the channel hot-carrier stressing conditions were harsh, they hardly had any effect on oxide integrity. Parenthetically, this result does

not support that oxide breakdown is due to interface state generation [3], since the stress condition is known to generate a large density of interface traps.

Channel Hot Carrier stressing with significant hole current

However, for devices operated with large amount of channel hot hole injection, the situation is different. In order to create a favorable electric field for hole injection, a high drain voltage ($V_D = 10 \text{ V}$) was applied to a long n-channel ($W/L = 100/10 \text{ in } \mu\text{m}$) thin gate oxide (90 \AA) MOSFET. Thin gate oxide is used in this experiment to increase the channel electric field [10] in order to produce large hole current. Because of the high oxide field near the drain when V_G is low, electrons can tunnel from gate to drain in addition to the channel hot hole injection into the gate. The electron tunneling current can be easily measured with the source floating. Fig.3a shows I_G and I_{SUB} as a function of V_G for such a device measured under normal and floating source conditions. The I_G curve with a peak at $V_G \approx 0.8 \text{ V}$ is under normal operation, while the other I_G curve, monotonically decreasing with V_G , is for floating source condition. The difference between these two cases is the contribution of channel hot-hole injection. Fig.3b shows the Q_{BD} of the devices after channel hot-carrier stressing for 2 hours.

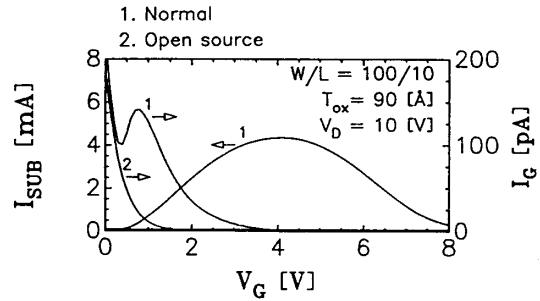


Figure 3a The I_G and I_{SUB} for a thin oxide (90 \AA) long channel ($W/L = 100/10 \text{ } \mu\text{m}$) MOSFET measured as a function of V_G at $V_D = 10 \text{ V}$. The gate current with a peak at $V_G \approx 0.8 \text{ V}$ is measured under grounded source (normal) condition, while the other I_G is measured with source floated. The difference between these two cases is due to channel hot hole injection.

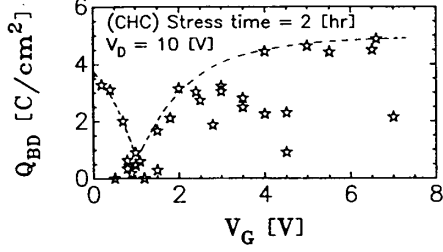


Figure 3b Q_{BD} data for the devices after having been stressed under the bias condition shown in Fig.3a for 2 hours. The scattering in Q_{BD} data is probably due to sample variations. However, no device shows high Q_{BD} value at $V_G \simeq 1V$, where hole injection is most efficient.

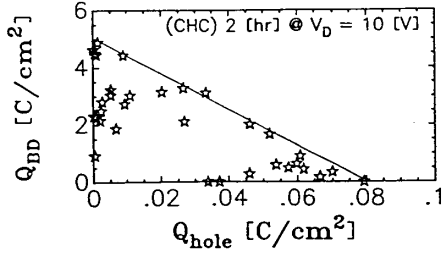


Figure 3c Replot the Q_{BD} data shown in Fig.3b in terms of the hole fluence, Q_{hole} , integrated during the channel hot carrier stressing. That all the Q_{BD} data fall within a triangle region suggests a linear correlation between hole fluence and Q_{BD} .

The small Q_{BD} and the large variation is due to the inferior oxide quality compared to the devices shown in Fig.2. However, there is a quite apparent drop in Q_{BD} at $V_G \simeq 1V$ where hole injection is most efficient. If the envelope of the Q_{BD} shown in Fig.3b represents the intrinsic breakdown of the devices, then the low values of Q_{BD} after channel hot carrier stressing at $V_G = 1V$ where the hole current peaks in Fig.3a support the correlation of hole current and oxide breakdown observed in other experiments [4,5]. This correlation can also be demonstrated by plotting the Q_{BD} data shown in Fig.3b as a function of hole fluence, Q_{hole} , which is obtained by integrating the gate current density with time during the channel hot carrier stressing, as shown in Fig.3c. In this figure, all the Q_{BD} data fall within a triangle region bounded by a line joining $Q_{BD} = 5 C/cm^2$ and $Q_{hole} = 0.08 C/cm^2$. This upper bound repre-

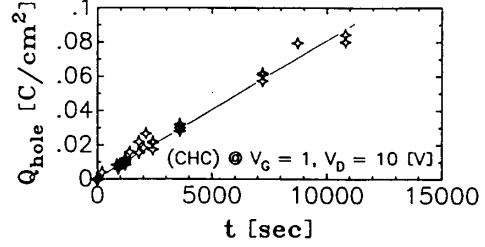


Figure 3d Hole fluence, Q_{hole} , as a function of time under the CHC stressing at $V_G = 1V$ and $V_D = 10V$ as shown in Fig.3a.

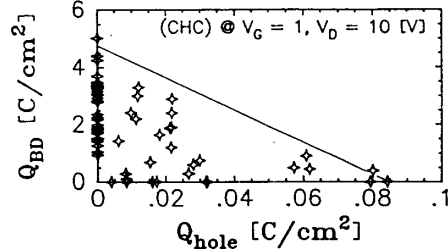


Figure 3e Q_{BD} data as a function of Q_{hole} after the stressing shown in Fig.3d. A similar triangle region to the one shown in Fig.3c further supports the correlation between oxide breakdown and hole fluence.

sents the effect of hole injection on intrinsic oxide integrity. All the other Q_{BD} data falling below the line are due to oxide defect to begin with. A similar experiment, i.e. CHC stressing at fixed V_G and V_D for various amount of time, can also produce this result. Fig.3d shows the Q_{hole} as a function of CHC stressing time at $V_G = 1V$ and $V_D = 10V$, and Fig.3e shows the Q_{BD} measured afterward as a function of the hole fluence injected. The similarity between Fig.3c and Fig.3e further supports the correlation of hole fluence and oxide breakdown.

Fig.3c and Fig.3e seem to set a stringent constraint on the number of hot-hole erasures a non-volatile memory cell can withstand. However, if each erasure requires a few times of $10^{-6} C/cm^2$ of holes and the effect of each erasure is additive, then according to Fig.3c the number of hot-hole erasures can be as high as a few times of 10^4 cycles, which is quite sufficient for many applications.

Snap-back Induced Gate-to-Drain Breakdown

It has been reported that when a MOSFET is biased into snap-back region, destructive gate oxide breakdown can occur between gate and drain [11]. This is a reliability concern for the ESD at the output devices and input protection circuits where MOSFETs are driven into snap-back by high voltage pulses. Since channel hot hole injection is more favorable at low gate voltages (holes are attracted to the gate), we thus suspect that the snap-back induced gate-to-drain breakdown could also result from hot hole injection.

Fig.4a shows the I_G and I_D of a 230 Å gate oxide device ($W/L = 5/3$) as a function of drain voltage with fixed gate voltage of 0.5 volt under normal or floating source conditions. For the normal case, the snap-back breakdown at about $V_D = 19.5$ volts is indicated by the sudden rise of I_D . While the gate current starts to show up at about $V_D = 17$ volts and also increase very abruptly at the snap-back. The sign of the gate current indicates hole injection from the channel or electron tunneling from the gate.

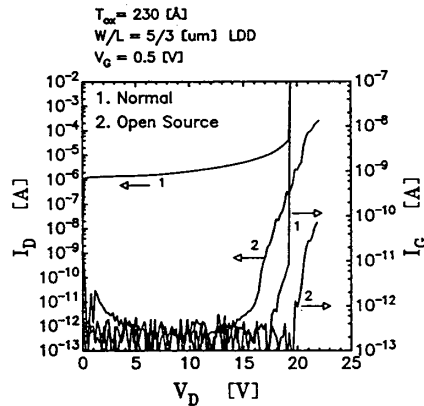


Figure 4a The gate current, I_G , and drain current, I_D , of a 230 Å gate oxide LDD device ($W/L=5/3$) as a function of V_D under grounded source (normal) or floating source conditions. ($V_G = 0.5$ volt) Under normal condition, snap-back occurs at $V_D = 19.5$ volts which is manifested by the sudden increase of I_D and I_G . The floating source measurement confirms that the I_G in the snap-back is not due to electron tunneling from gate to drain.

Since no electron tunneling from gate to drain is observed until $V_D = 20$ volts (Fig.4a), we know that the gate current in Fig.4a is due to channel hot hole injection.

The snap-back can be instantaneously destructive and cause gate-to-drain short if the limit of the drain current supply is relatively high (e.g. 10 mA). In order to prolong the damaging process, a constant current of 10^{-4} A is applied to the drain to bias the transistor at the onset of snap-back. Fig.4b shows the time evolution of V_D and I_G under stressing in this snap-back condition. The gradual increase of drain voltage necessary to maintain a constant snap-back current of 10^{-4} A is due to hole trapping in the oxide near the drain in the well known manner of “walk-out”. The decrease of gate hole current with time is also due to hole trapping, which retards further hole injection. Eventually the gate current becomes unstable and starts to rise and the drain voltage starts to fall. The stressing is stopped at this point. Fig.4c compares the F-N tunneling I-V curve of the device after the snap-back stressing to that of a fresh device. The I-V curve for the stressed device begins to the left of the fresh one, crosses the fresh device curve at about $I_G = 3 \times 10^{-12}$ A, and eventually becomes parallel to the fresh I-V curve indicating net electron traps are generated. This is, however, as expected since it is known that electron

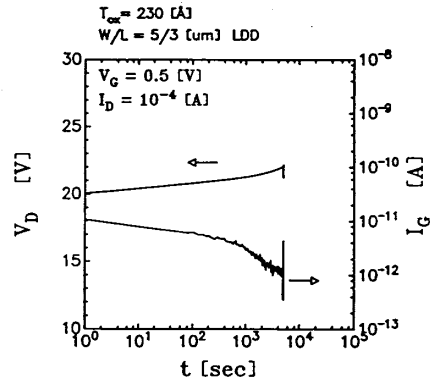


Figure 4b The drain voltage, V_D , and gate current, I_G , as a function of time during a constant snap-back current stressing of $I_D = 10^{-4}$ A.

traps can be generated by recombination of holes and electrons in the oxide [12]. The relatively large recombination, and thus trap generation, capture cross section, about 10^{-14} cm^2 , can explain the low current at which those two I-V curves cross (Fig.4c). The parallel I-V shift to the right of the fresh one is either due to trapped electrons or simply due to reduced charge-free area near the source side. The final current in the I-V curves before breakdown, I_{gBD} , is also lower for devices with snap-back stress, which again indicates that gate oxide integrity is degraded. Fig.4d show the I_{gBD} as a function of the hole fluence injected during the snap-back stress, Q_{hole} . The fact that I_{gBD} decreases with increasing Q_{hole} once again supports that hole injection degrades gate oxide integrity.

Summary

The effects of channel hot-carrier stressing on gate oxide integrity results from channel-hot hole injection. Devices stressing without directly measurable hole current, such as the typical channel hot carrier (CHC) stressing, has no significant effect on oxide integrity, despite the large ΔV_T and $\Delta I_D/I_D$ degradation resulting from the CHC stressing. However, for thin gate oxide devices operated at $V_G \approx V_T$ and very high V_D , large gate hole current may be observed and there is a linear correlation between the hole fluence during the CHC stressing and the oxide charge-to-breakdown measured afterwards. For every 0.01 C/cm^2 of hole fluence, Q_{BD} is reduced by about 1 C/cm^2 . The maximum hole fluence a MOSFET can withstand before the oxide breakdown was found to be about two orders of magnitude smaller than the F-N tunneling electron fluence that the gate oxide can withstand. The snap-back induced gate-to-drain breakdown observed in ESD protection devices [11], can also be explained by this model. For stressing in the snap-back regime, we have also found a linear correlation between hole fluence and Q_{BD} . Stressing in the snap-back regime can cause oxide breakdown in a short time because the field condition in grounded gate snap-back is highly favorable for hole injection currents. These

results support the belief that oxide breakdown is caused by hole flow and perhaps trapping instead of interface state generation or electron trapping since, without significant amount of hole fluence, Q_{BD} is independent of ΔV_T or $\Delta I_D/I_D$, which are generally believed to be associated with interface state generation or electron trapping. Oxide integrity degradation should not be a concern under the usual hot-carrier stressing condition where I_{SUB} is at a maximum.

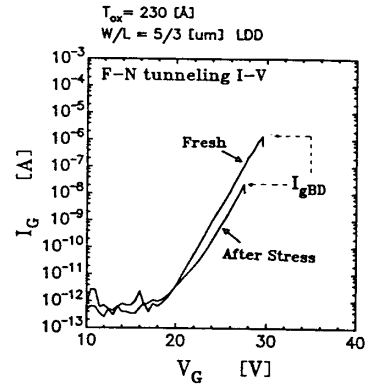


Figure 4c The F-N tunneling I-V curves of a fresh device and a device experienced the previous snap-back stressing. The crossing of the stressed I-V curve and the fresh one at $I_G \approx 3 \times 10^{-12} \text{ A}$ is due to electron trap generation [12]. The oxide integrity degradation for the stressed device is evidenced by the lowering of breakdown current. The sudden drop, instead of rise, of current at oxide breakdown is due to burning open the thin poly and/or metal line.

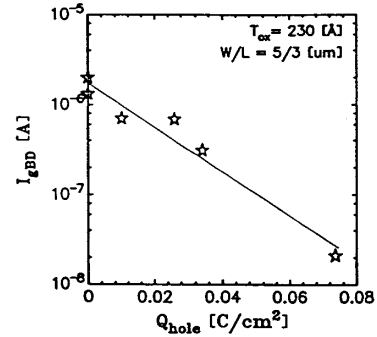


Figure 4d Breakdown current, I_{gBD} , in the previous ramp-voltage I-V measurement as a function of hole fluence, Q_{hole} , injected during the stressing. The decreasing of I_{gBD} with Q_{hole} once again demonstrates the correlation of hole fluence and oxide breakdown.

Acknowledgment

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