CIRCUIT RELIABILITY SIMULATOR - OXIDE BREAKDOWN MODULE

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ABSTRACT

A computer program which generates statistics about circuit failures due to MOS oxide breakdown has been developed. The program, CORS (Circuit Oxide Reliability Simulator), predicts the probability of circuit failure as a function of operating time, temperature, power supply voltage and input waveforms. It consists of a pre- and post-processor for SPICE. CORS calculates the probability of failure by using the node voltages provided by SPICE and oxide defect statistics which are provided by the user. The effect of burn-in on oxide reliability can also be simulated. CORS is linked to a hot electron and an electromigration reliability simulator.

INTRODUCTION

Circuit failure due to oxide breakdown may ultimately limit one's ability to scale down MOS devices without changing the power supply voltage. CORS helps determine if the oxide quality for a particular process is high enough to meet the specified lifetime under expected operating conditions with a low failure rate. This program is part of a larger reliability software package containing the hot electron aging simulator named CAS [1] and an electromigration failure simulator [2].

The CORS user creates an input deck similar to an ordinary SPICE input deck with a few additional commands which are used to tailor the oxide breakdown simulation. The user is also required to provide the ramp voltage breakdown statistics or the time to breakdown statistics of test capacitors. The simulator uses this supplied data to derive the oxide defect distribution for the particular technology.

OXIDE BREAKDOWN MODEL

Oxide intrinsic lifetime is [3]

$$t_{BD} = \tau(T)\exp(\frac{G(T)X_{ox}}{V_{ox}}) \quad (1)$$

where t_{BD} is the time to breakdown, $\tau(T)$ and $G(T)$ are the temperature dependent intercept and slope of the $\ln(t_{BD})$ vs $\frac{1}{E}$ plot, X_{ox} is the oxide thickness, and V_{ox} is the voltage across the oxide (which may differ from the applied voltage due to the work function difference between the electrodes). Figure 1 illustrates the validity of Equation (1) [4]. We believe that the $\frac{1}{E}$ dependence of t_{BD} comes from its dependence on the Fowler-Nordheim tunneling current and the hole generation efficiency, both of which vary as $exp(\frac{-1}{E})$ [3]. Large area samples breakdown at a wide range of (shorter) times due to oxide defects.

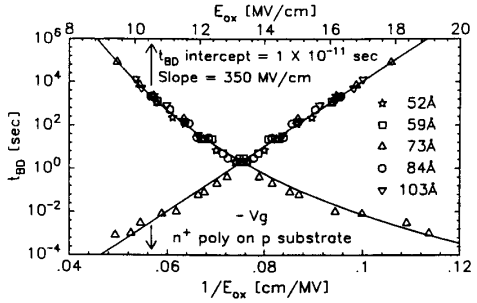

Figure 1. $\ln(t_{BD})$ vs $\frac{1}{E_{ox}}$ and E_{ox}. It appears that the data has a $\frac{1}{E_{ox}}$ dependence.

Defects, of many hypothetical natures, may be modeled by a random variable X_{eff} ("effective thickness"), where $X_{eff} \leq X_{ox}$, and an area density, $D(X_{eff})$ [5]. Breakdown is predicted to occur at

$$t_{BD} = \tau(T)\exp(\frac{G(T)X_{eff}}{V_{ox}}) \quad (2)$$

The probability that an oxide breaks down at or before a specified time, t, is [6]

$$P(t_{bd} \leq t) = 1-\exp(-AD(X_{eff})) \quad (3)$$

where X_{eff} satisfies equation (2) for t_{BD} equal to t, A is the oxide area and defects are assumed to be uniformly distributed across the wafer. Non-uniform defect distributions, such as the gamma distribution, can also be accommodated. Equation (3) may be used to directly derive $D(X_{eff})$ from test capacitor time to failure statistics (Figure 2). $D(X_{eff})$ can also be derived from the quicker ramp voltage breakdown test (Figure 3) by making use of the following equation [7],

$$1 = \frac{{V_{bd}}^2}{RG(T)\tau(T)X_{eff}} exp(\frac{-G(T)X_{eff}}{V_{BD}}) \quad (4)$$

along with equation (3). Both types of failure statistics data should yield identical $D(X_{eff})$ (Figure 4). The validity of the X_{eff} model is illustrated in Figure 5 where the distribution of $D(X_{eff})$ derived from data taken at 8V and 25C was used to successfully predict experimental results at a variety of test voltages and temperatures.

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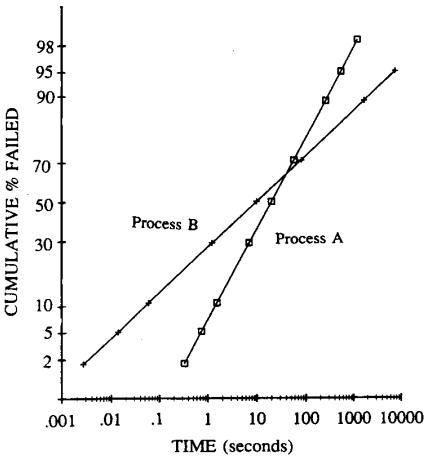


Figure 2. $D(X_{eff})$ can be derived from lifetime data.
Process A: $t_{50} = 20$, $\sigma = 2$
Process B: $t_{50} = 10$, $\sigma = 4$

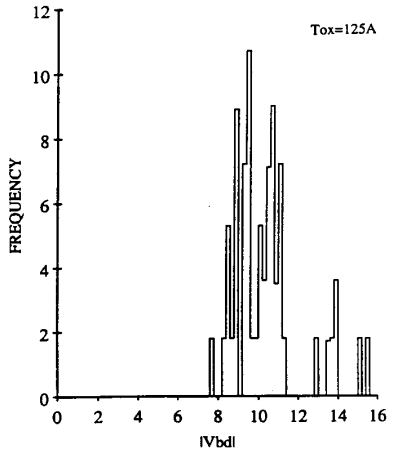


Figure 3. $D(X_{eff})$ can be derived from test capacitor ramp breakdown data such as this.

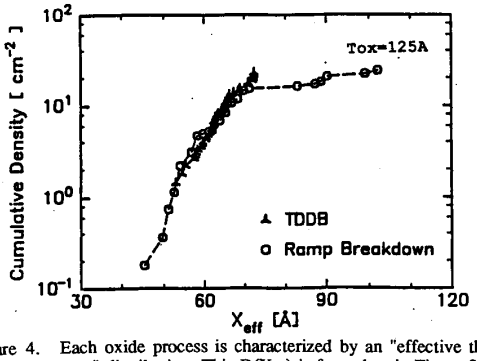


Figure 4. Each oxide process is characterized by an "effective thickness" distribution. This $D(X_{eff})$ is from data in Figure 2.

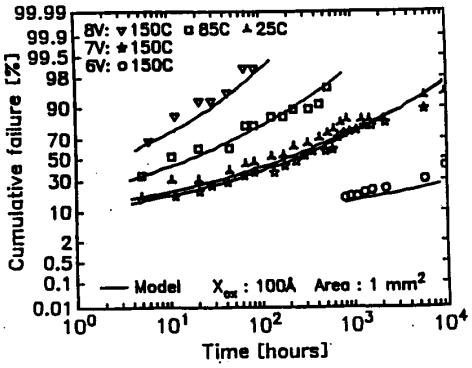


Figure 5. Experimental data fits X_{eff} model predictions.

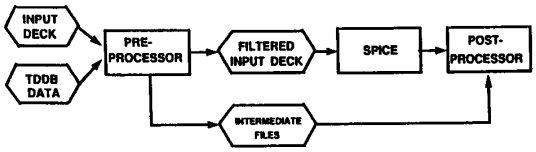


Figure 6. Block diagram of oxide reliability simulator.

MODEL IMPLEMENTATION

Inside a circuit environment, oxides generally do not see a constant field, but rather a time-varying one. Using a quasi-static approach, we derive an equation for oxide breakdown in the presence of a time-varying field. After some amount of damage has been sustained by an oxide, it will break down. We assume that this amount of damage, which will be referred to as " Δ_{BD} ", is a constant [5]. It follows that

$$d\Delta \propto exp(\frac{-GX_{eff}}{V_{ox}(t)})\, dt \tag{5}$$

$$\Delta_{BD} = \int_0^{t_{BD}} \exp(\frac{-GX_{eff}}{V_{ox}(t)})\, dt = Constant \tag{6}$$

If $V_{ox}(t)$ is constant, the above reduces to

$$exp(\frac{-GX_{eff}}{V_{ox}})t_{BD} = Constant \tag{7}$$

By comparison with equation (2), we see that the constant must be equal to τ. The final result is

$$1 = \frac{1}{\tau}\int_0^{t_{BD}} \exp(\frac{-GX_{eff}}{V_{ox}(t)})\, dt \tag{8}$$

Experiments indicate that this quasi-static approach produces conservative lifetime predictions [8].

CORS determines $V_{ox}(t)$ for each oxide element in the circuit from the SPICE node voltages and a consideration of the work function difference between the electrodes. Figure 6 shows a block diagram of the system. Circuit failure statistics are calculated using the rule that if any MOSFET or capacitor experiences breakdown, then the entire circuit fails. The probability

that a particular device fails is given by equation (3). Device failures are treated as independent events and the net probability of failure is given by

$$P(circuit\ failure) = 1 - \prod_{i=1}^{\#\ devices} \exp(-A_i D(x_{eff_i})) \qquad (9)$$

Simulation accuracy increases if the user provides separate data files for NMOS, PMOS, diffusion edge and field edge test structures. The simulator can accept these breakdown statistics in the form of empirical data (preferred for accuracy) or, where data is not available, in the form of parameters for single or multiple population Lognormal and Weibull distributions.

SIMULATION RESULTS

The remaining figures highlight the capabilities of CORS. All simulations were performed for CMOS circuits operating at 5.5V and 125C, unless otherwise stated. Figure 7 shows the dramatic effect of oxide quality on the expected circuit lifetime of a 10K gate array operating at 12.5MHz (gates are 4-input nands). The lifetime curves in Figure 7 correspond to the Process A and Process B defect distributions as plotted in Figure 2. Figure 8, for the same circuit, shows that the inclusion of edge defects can change the predicted lifetime depending on the relative density and severity of the edge defects.

Figure 9 and Table 1 highlight the dependence of oxide degradation on input waveforms. Input waveforms are seen to greatly influence which devices in a circuit are most likely to fail. Note that CORS has an option for printing out the breakdown probability for individual devices. This feature will be useful in helping to identify the devices causing most failures.

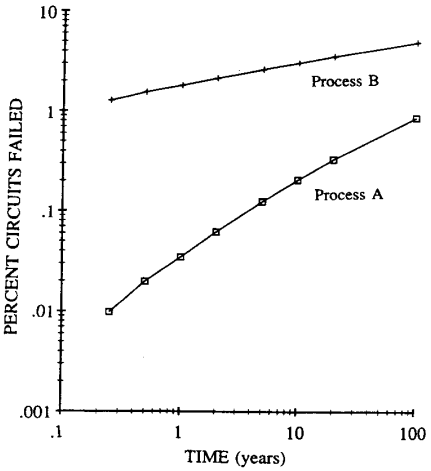


Figure 7. Predicted oxide failure of a 10K gate array at 12.5 MHz.

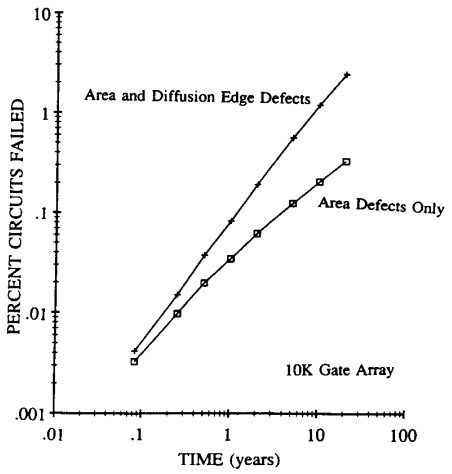
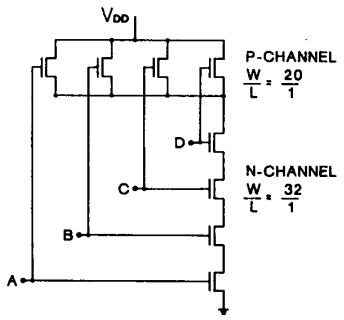


Figure 8. NMOS, PMOS, field or source/drain edges can have different defect distributions.



	C varying	A & C varying
MNA	1.85×10^{-6}	1.48×10^{-6}
MNB	1.85×10^{-6}	1.71×10^{-6}
MNC	1.05×10^{-6}	1.05×10^{-6}
MND	1.07×10^{-6}	1.06×10^{-6}
MPA	0.0	6.28×10^{-7}
MPB	0.0	0.0
MPC	8.20×10^{-7}	6.26×10^{-7}
MPD	0.0	0.0

Figure 9 and Table 1.
Failure probability of individual devices can be listed to identify the most susceptible devices (tabled probabilities calculated at 10 years operation).

Figure 10 shows simulated reliability after burn-in for a variety of burn-in power supply voltages, temperatures and durations. The defect distribution used for this simulation is that shown in Figure 4. These studies are useful for balancing conflicting goals such as cost, avoidance of hot electron degradation and reduction of field failures due to oxide breakdown in choosing the burn-in condition for a product.

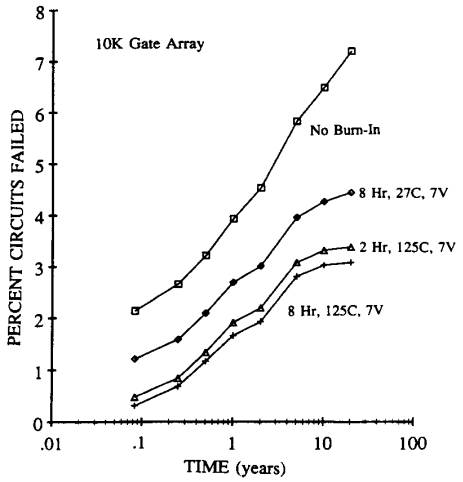


Figure 10. The simulator can simulate the effect of burn-in on circuit reliability.

Figures 11 and 12 show the effects of memory size and operating temperature on the reliability of SRAM cell arrays. The circuit was simulated for read operations only. Simulations were performed for a SRAM cell in the idle state as well as one undergoing continuous precharge and read operations. Both cells have nearly identical failure statistics. The simulator showed that under each of these conditions the same two transistors in the SRAM cell dominate circuit breakdown. The oxide field across those two transistors does not change appreciably during a read operation.

For simple simulations, those where the user does not request burn-in and does not include edge defects, CORS predicts circuit failure probabilities of the same order of magnitude as one gets by simply assuming that all MOS devices have the power supply voltage applied across the oxide at all times. However, CORS can also do calculations which are too cumbersome to work without a computer, such as reliability after burn-in predictions. By using the SPICE generated node voltages, CORS also gives the designer a feel for which specific devices will be the ones likely to fail, something which is lost by assuming that all devices see the maximum field all of the time.

CONCLUSIONS

CORS has been developed to predict failure probabilities of MOS circuits as a function of time and operating conditions. CORS is also a tool for optimizing burn-in. CORS will help circuit designers determine if a particular design is feasible for a given process.

ACKNOWLEDGMENTS

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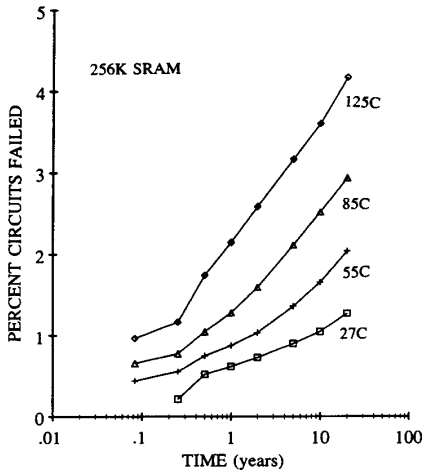

Figure 11. Simulated failure rate of an SRAM.

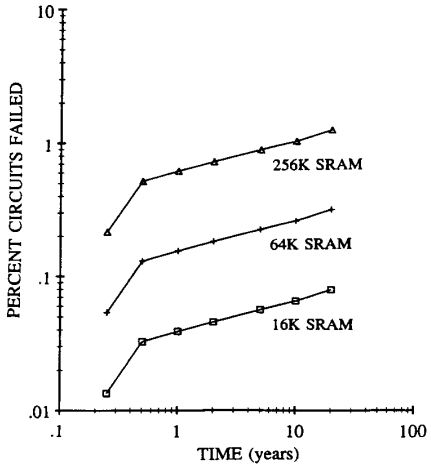

Figure 12. Effect of temperature on failure rate.

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