A PHYSICAL MODEL FOR MOSFET OUTPUT RESISTANCE

J. H. Huang, Z. H. Liu, M. C. Jeng*, P. K. Ko, C. Hu
Department of Electrical Engineering and Computer Sciences
University of California, Berkeley, CA 94720
*Cadence Design System, Santa Clara, CA 95054

Abstract—The output resistance \( R_{out} \) is one of the most important device parameters for analog applications. However, it has been difficult to model \( R_{out} \) correctly. In this paper, we present a physical and accurate output resistance model that can be applied to both long-channel and submicrometer MOSFETs. Major short channel effects and hot-carrier effect, such as channel-length modulation (CLM) [1], drain-induced-barrier-lowering (DIBL) [2] [3] [4] and substrate current induced output resistance reduction [5] [6], are all included in this model, and it is scalable with respect to different channel length \( L \), gate oxide thickness \( T_{ox} \), and power supply \( V_{dd} \). This model can be incorporated into existing MOSFET's model without introducing discontinuity.

I. INTRODUCTION

In analog circuit applications, the voltage gain is directly proportional to \( R_{out} \). Existing analytical models for MOSFET \( R_{out} \) are not adequate [7], because only channel-length modulation effect is included. The empirical model[6] is more accurate, however it lacks scalability. To achieve high accuracy and scalability, \( R_{out} \) model must be analytical and include all the major physical mechanisms that affect \( R_{out} \). The typical MOSFET I-V characteristic and output resistance are shown in Fig. 1.

![Fig. 1. Typical drain current and output resistance.](image)

\( \frac{W}{L} = 10 / 0.43 \), \( T_{ox} = 75 \text{Å} \).

\[ I_{ds}(V_{gs}, V_{ds}) = I_{ds}(V_{gs}, V_{ds}) = \alpha \frac{d I_{ds}(V_{gs}, V_{ds})}{d V_{ds}} (V_{ds} - V_{ds}) \]
\[ = I_{ds} (1 + (V_{ds} - V_{ds})/V_{A}) \]

where \( V_{ds} \), \( V_{gs} \), and \( V_{ds} \) are the saturation voltage and is given by
\[ V_{ds} = E_{sat} L V_{gs} + (E_{sat} L + V_{gs})/2, \quad V_{sat} = 2 V_{gs} \mu_{eff} C_{ox}, \quad V_{s} \]

and \( \mu_{eff} \) are saturation velocity and mobility, respectively.

\[ I_{ds} = I_{ds}(V_{gs}, V_{ds}) = \alpha_{sat} W C_{ox} (V_{gs} - V_{ds}) \]

\[ W \] is the width, and \( C_{ox} \) is gate oxide capacitance. \( V_{A} \) has three components, i.e., \( V_{CLM} \), \( V_{ADIBL} \), and \( V_{ASCBE} \), corresponding to CLM, DIBL, and SCBE, respectively. Each component can be evaluated separately.

\[ \frac{1}{V_{A}} = \frac{1}{I_{ds}} ((\frac{d I_{ds}}{d V_{ds}})_{CLM} + \frac{d I_{ds}}{d V_{ds}})_{DIBL} + \frac{d I_{ds}}{d V_{ds}})_{SCBE} \]
\[ = \frac{1}{I_{ds}} + \frac{1}{V_{CLM}} + \frac{1}{V_{DIBL}} + \frac{1}{V_{ASCBE}} \]

(i) Channel Length Modulation (CLM)
As \( V_{ds} > V_{ds} \), the velocity saturation region near the drain extends toward the source, which reduces the effective channel length and in turn increases the drain current. The channel length reduction \( \Delta L \) satisfies \( V_{ds} = V_{ds} + I_{ds} \sin(\Delta L/\ell) \)

[1], where \( \ell = \sqrt{W_{ox} X_{j}} \) . \( X_{j} \) is the channel depth. \( V_{ds} \) is a
function of $L - \Delta L$, therefore is a function of $V_{ds}$. $V_{ACLM}$ can be calculated by

$$\frac{1}{V_{ACLM}} = \frac{1}{I_{ds}} \left( \frac{\partial I_{ds}}{\partial V_{ds}} \right)_{V_{GC}} = \frac{1}{I_{ds}} \left( \frac{\partial I_{ds}}{\partial V_{ds}} \frac{\partial V_{ds}}{\partial L} \frac{\partial L}{\partial V_{ds}} \right)$$

(3)

We can obtain

$$V_{ACLM} = (E_{sat} + V_{gss})/(V_{ds} - V_{dss})/E_{sat}$$

(4)

where $V_{gss} = V_{gs} - V_{th}$.

(ii) Drain Induced Barrier Lowering (DIBL)

As $V_{ds}$ is applied to the drain, the barrier height between the source and drain will be lowered[2][4][6], therefore the threshold voltage $V_{th}$ is reduced and in turn the drain current increases. It has been shown[4] that threshold voltage reduction due to DIBL is given by $\theta(L)V_{ds}$. $\theta(L)$ is the DIBL coefficient which has strong dependence on the channel length and is given by

$$\theta(L) = \exp(-L/2l) + 2\exp(-L/l)$$

(5)

where $l = \sqrt{3}t_{ox}X_{dep}/\eta$ and $X_{dep}$ is the depletion width at the source, and $X_{dep}/\eta$ is the average depletion depth along the channel, where $\eta$ is determined by experimental data. $V_{ADIBL}$ can be evaluated by

$$\frac{1}{V_{ADIBL}} = \frac{1}{I_{ds}} \left( \frac{\partial I_{ds}}{\partial V_{ds}} \right)_{DIBL} = \frac{1}{I_{ds}} \left( \frac{\partial I_{ds}}{\partial V_{ds}} \frac{\partial V_{ds}}{\partial V_{th}} \frac{\partial V_{th}}{\partial L} \right)$$

(6)

From the above argument, we obtain

$$V_{ADIBL} = (E_{sat}L + V_{gss})/\theta(L)(1 + 2E_{sat}L/V_{gss})$$

(7)

(iii) Substrate Current Induced Body Effect (SCBE)

At even higher $V_{ds}$, the electrical field near the drain becomes very high (>0.1MV/cm), some electrons traveling through this region will acquire enough energy to cause impact ionization and result in substrate current. The substrate current will flow through the substrate, produce an ohmic drop across the substrate resistance $R_{sub}$, and increase the substrate potential. This substrate potential will reduce $V_{th}$ and hence increases the drain current. On the other hand the electrons (in NMOS) created during impact ionization will go into the drain directly. Therefore we have

$$V_{SCBE} = \frac{1}{R_{sub}} \left( 1 + \frac{\gamma}{2\sqrt{\eta}} - V_{th} \right) \left[ \frac{R_{sub}}{V_{ds} - V_{dss}} \right] \exp(\frac{-R_{sub}}{V_{ds} - V_{dss}})$$

(8)

where $A$ and $R_{sub}$ are the parameters associated with the substrate current determined by experimental data [5]. $\gamma$ is the transconductance, $\gamma$ is the coefficient of body effect, $V_{th}$ is the surface potential. $V_{SCBE}$ has very strong dependence on $V_{ds}$.

This is because substrate current depends on $V_{ds}$ exponentially [5]. In order to make the drain current and the first order derivative continuous at $V_{ds} = V_{dss}$, and also take into account LDD structure effect on $V_{out}$, Eq. (2) is modified as

$$V_{out} = V_{A} + (1 + \alpha L_{ox}/(V_{V_{ACLM}} + V_{ADIBL} + V_{SCBE}))$$

(9)

where $V_{out}$ is the Early voltage at $V_{ds} = V_{dss}$, which can be obtained from the triode region. $L_{ox}$ is the length of LDD region. The term $\alpha L_{ox}/(V_{V_{ACLM}} + V_{ADIBL} + V_{SCBE})$ takes into account the LDD structure effect on $R_{out}$[4]. $\alpha$ will be extracted from experimental data. If the triode region current model in [1][8] is used, then

$$V_{out} = E_{sat}L + V_{dss}$$

The formulation ensures that $R_{out}$ is continuous throughout all regions, which is an important property for robust circuit simulations. Because the Early voltage approach for modeling $R_{out}$ does not depend on the specific form of the drain current. This methodology is suitable to any MOSFET's model.

III. RESULTS AND DISCUSSION

The individual component of $V_{A}$ together with the resultant $V_{A}$ are shown in Fig. 2. The dominant mechanism is the one with the smallest Early voltage in each region.

![Fig. 2. Early voltage and its components versus $V_{ds}$](image)

Fig. 3 shows measured $R_{out}$ and the model at different gate voltages. The good agreement between experimental data and modeling results makes the model highly suitable for analog applications. Quantitatively predicting the scaling effects on $R_{out}$ can also be done. Figs. 4 and 5 show $R_{out}$ versus $V_{ds}$ for various channel lengths and gate oxide thicknesses, respectively. The most important characteristics of $R_{out}$ in circuit designs are the maximum $R_{out}$ which determines the maximum available gain from the device, and the onsets of drain voltage at which $R_{out}$ starts
decreasing on both sides of the maximum $R_{out}$, which determines the dynamic swing of the drain voltage.

![Graph 3: NMOS $R_{out}$ versus $V_d$ at different gate voltage](image)

**Fig. 3.** NMOS $R_{out}$ versus $V_d$ at different gate voltage

![Graph 4: $R_{out}$ versus $V_d$ for different channel length. Gate voltage is 0.5V above threshold voltage](image)

**Fig. 4.** $R_{out}$ versus $V_d$ for different channel length. Gate voltage is 0.5V above threshold voltage.

![Graph 5: $R_{out}$ versus $V_d$ for different gate oxide thickness](image)

**Fig. 5.** $R_{out}$ versus $V_d$ for different gate oxide thickness.

Among the three mechanisms stated above, DIBL has the greatest impact on the maximum $R_{out}$, while SCBE and $V_{doff}$ limit the dynamic range of $V_d$. Fig. 4 shows that maximum $R_{out}$ is reduced as channel length decreases, this is because CLM and DIBL effects become more severe as channel length is reduced. The channel length sensitivity of maximum $R_{out}$ is mainly due to the exponential dependence of $\theta(L)$ on channel length [4]. $\theta(L)$ and maximum $R_{out}$ versus channel length and gate oxide thickness are shown in Fig. 6 and 7, respectively.

![Graph 6: DIBL coefficient $\theta(L)$ versus channel length. $W = 10 \mu m$](image)

**Fig. 6.** DIBL coefficient $\theta(L)$ versus channel length. $W = 10 \mu m$

![Graph 7: Maximum $R_{out}$ versus channel length. $W = 10 \mu m$](image)

**Fig. 7.** Maximum $R_{out}$ versus channel length. $W = 10 \mu m$

As gate oxide thickness decreases, short channel effects are suppressed and maximum $R_{out}$ increases, as shown in Fig. 5. However, the substrate current induced body effect (SCBE) is also enhanced as indicated by the faster $R_{out}$ decreasing in the high field region for device with thinner $t_{ox}$. It is interesting to note that, for a given technology, the hot-carrier effects (e.g. SCBE) will be enhanced when the short channel effects (e.g. CLM & DIBL) are suppressed, or
vice versa, except for the introduction of LDD which improves both. This is because when the short channel effects are to be suppressed, the high field region has to be shortened. Therefore the maximum lateral electrical field is increased and hot-carrier effects is enhanced.

If we assume that the minimum $R_{\text{out}}$, required in a design is 120 kohms, a contour of the drain voltage and channel length at which $R_{\text{out}}=120$ kohms can be plotted as shown in Fig. 8. The regions enclosed by the contour represent the acceptable design windows. The dynamic swing for any given channel length can be clearly determined from Fig. 8. As expected, devices with thicker gate oxide will provide larger voltage swing, because of weaker SCBE, but the minimum channel length which can be used is also longer due to worse short-channel effects. With this model, families of plots similar to Fig. 8 at different $V_{\text{gs}}$ can be generated and used by analog circuit designer in choosing the optimal device dimensions and bias conditions.

![Fig. 8. Contours of $R_{\text{out}}$ equal to 120KΩ.](image)

Figs. 9 and 10 show that $R_{\text{out}}$ model also has capability of modeling PMOS and LDD MOSFET.

![Fig. 9. Output resistance modeling for PMOS.](image)

![Fig. 10. Output resistance for LDD device.](image)

### IV. CONCLUSIONS

A physical-based analytical model for MOSFET output resistance is presented. Major physical mechanisms important to the output resistance are considered and analyzed. Scaling effects of channel length, gate oxide thickness and power supply on the output resistance are also investigated. This model can be incorporated into any exist MOSFET’s model without introducing discontinuity.

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