Comparison of Electromigration Reliability of Tungsten and Aluminum Vias Under DC and Time-Varying Current Stressing

Jiang Tao, K. K. Young*, Nathan W. Cheung, and Chenming Hu

Department of Electrical Engineering and Computer Sciences
University of California, Berkeley, CA 94720

*Circuit Technology Research and Development
Hewlett Packard Company, Palo Alto, CA 94304

Abstract

Using Kelvin test structures, the via reliability with respect to electromigration failure of tungsten and aluminum vias under DC, pulse-DC and AC stressing have been studied. Our results indicate that although W-plug vias can eliminate the step coverage problem, this metallization system is not ideal because the Al/W contact represents an undesirable flux divergence location for electromigration. Al vias are more reliable than W-plug vias with respect to electromigration failure. The via lifetimes under bidirectional stressing current are found to be orders of magnitude longer than DC lifetimes under the same stressing current density for both W and Al vias. The unidirectional 50% duty-factor pulse-DC lifetime is found to be twice the DC lifetime at low frequency region (<200Hz) and 4-5 times the DC lifetime at high frequency region(>10KHz), in agreement with the vacancy relaxation model.

Introduction

CVD tungsten and selective tungsten deposition have been widely investigated for forming plug vias and interconnects in ULSI circuits to improve the planarity of metallization system [1-2]. Aluminum interconnect system is the metal system best understood and most commonly used at the present. Its relatively low resistivity gives it the advantage with respect to RC delay. While W plug technology is more widely studied, there continues to be interest in using Al for future generation via technologies[3-4]. Although extensive studies of electromigration failure of aluminum interconnects have been reported, few reports are available on the reliability of vias[5-8]. In addition, to our knowledge, no data has been reported for electromigration performances of vias under time-varying current conditions even though integrated circuits usually operate under time-varying and bidirectional current conditions. Experiments have shown that high-frequency currents cause different electromigration characteristics with respect to those induced by continuous currents in metal interconnects[9]. The objective of the present study is to determine the via reliability with respect to electromigration failure for both W and Al via systems under continuous and time-varying current stressing conditions. The potential reliability problem of Al/W via contacts is presented.

Experiment

In this study a single four-terminal Kelvin-contact test structure was chosen for investigation of the electromigration performances of vias although via chain structures were also tested. In other words, the study emphasizes the "intrinsic" behavior rather than the statistical distributions. Using the Kelvin structure, the via resistance and the interconnect resistance can be monitored separately and whether an open failure has occurred at the via or in the interconnect can be determined. In our test structures as shown in Table I, the first level metal(M1) consists of sputtered TiW(1500Å) / Al-Cu(4wt%)(5000Å) / TiW(700Å) multilayer metals(from bottom to top). Vias were opened in the 7000Å thick interlevel SiO_2 by standard photolithographic and dry etching techniques. For Al vias, a three step etching process was used to obtain a sloped profile and to minimize the critical dimension loss. The last step of the process etched away the top TiW layer of metal 1 from the bottom of the via hole, and the slope after etching is about 60°. Fig.1 shows the TEM(cross-section) micrograph of the Al-via structure. For W vias, on the other hand, the via hole wall was essentially vertical, and the tungsten plugs were selectively deposited in the via holes before M2 was sputter-deposited. During the via hole etching process, the top TiW layer of metal 1 was also mostly etched away from the bottom of the via hole with perhaps only 100Å of TiW left. The final via area is $0.7\times0.7\mu m^2$. The second level metal(M2) structure of structure C is exactly the same as M1 while structure A and B do not have bottom TiW in M2, and the thickness of different layer is also the same as that of M1. All the metal layers were deposited by using conventional sputtering methods. After M2 patterning all the wafers were passivated with 5000Å of TEOS.

A current source regulated by a transistor and driven by the output of a TTL gate was used to generate pulse DC and AC current signals [10]. Electromigration testings were performed on wafers placed directly on the heated stage of a probe station. Before electromigration testing, the temperature coefficient of via resistance was obtained in order to determine the temperature rise at vias due to self heating under high current density stressing. For continuous DC electromigration testing, the vias were stressed with a current density (current divided by the via area) of $3.5\times10^7 A/cm^2$ and $4.5\times10^7 A/cm^2$. During pulse - DC

CH3084-1/92/0000-0338$01.00 © 1992 IEEE/IRPS

electromigration testing, the rectangular pulsed DC waveform of peak current density 4.5×10^7A/cm^2 and duty factor of 50% in the frequency range of 0.5Hz to 1MHz was used. Finally for AC testing, a rectangular waveform was used having a peak current density of 4.5×10^7A/cm^2 and duty factor of 50% at 1MHz. All electromigration testings were carried out at an ambient temperature of 250°C. Via resistance was monitored periodically during testing. Device failure was defined to be a complete open. The median-time-to-failure(MTTF) was found by assuming a log-normal failure distribution and performing a linear regression.

Results and Discussion

DC Stressing

The effects of electron flow direction passing through the vias on the MTTF under continuous current signals for different structures are shown in Table I. The failure locations were easily identified from the electrical connectivity among the four Kelvin leads and sometimes confirmed with scanning electron microscopy(SEM). No failure of any Al via (structure A) was observed before the interconnects became open as shown in Fig.2. The interconnect lifetimes are about 8 hours for structure A, which represent the low limit of the actual Al-via lifetime. The lifetimes of Al vias are not only longer than the lifetimes of W-plug vias(structure B), but also longer than that of interconnects, even though the current density passing through the vias is more than 10X higher than the current density passing through the interconnects. This surprising result can be explained by the small via volume which may not contain any bad Al atom flux divergence point(e.g. single Al-grain), because the via area in our case is smaller than Al grain size. The Al flux flow is continuous through the via. The shorter lifetime of W-plug vias is because W has very high electromigration resistance compared to Al, and Al/W contacts present a bad flux divergence location for Al electromigration [11].

Fig.3 shows the SEM(cross-section) micrograph of the failure of structure B when electron flow was from M2 to M1. Under this condition, because of electromigration induced mass transport, aluminum will pile up at the top of W-plug vias, while an aluminum depletion will develop at the bottom of the via area, as shown in Fig.4. The continuous pushing from the top of W-plug via(caused by the Al accumulation) and depleting of aluminum at the bottom of the via will cause W-plug to move towards the bottom M1 layer. The catastrophic failure due to W-plug movement as shown in Fig.3 can be attributed to the effects of current crowding and localized heating occurred at the via area under high current stressing. In our experiment, in order to get the lifetime in a reasonable length of time, the vias were stressed with a very high DC current density of 3.5×10^7A/cm^2. The via temperature due to joule heating was calibrated with via resistance and is found to be about 400°C(i.e. a temperature rise of 150°C).

The effects of the addition of TiW layer in W-plug vias can be seen by comparing structure B and C for electron flow from M1 to M2. For structure B, when electrons move from M1 to M2, aluminum will be pushed away from the top surface of the W-plug vias and voids will develop at the contact area, as shown in Fig.5. Fig.6(a) shows the scanning electron microscopy(SEM) micrograph of the via open failure in this case. Severe joule heating toward the end of electromigration test after Al has been pushed away from most of the plug top is believed to be responsible for the disappearance of the M2 layer over the via area. While for structure C, with electron flowing from M1 up to M2, the failure location was found in M2 lead in the vicinity of the via as shown in Fig.6(b). In this case, the bottom TiW layer of M2 served as a robust current spreader. Therefore, open failure did not occur at the via area even after Al has been pushed away from the plug area. This result indicates the addition of TiW layers next to W-plug can change the electromigration failure mode and improve its electromigration reliability.

Fig.7 shows the via resistance versus DC electromigration stressing time when electron flow was from M1 to M2. We can see the via resistances of W-plug vias are about 5-7 times larger than that of Al-vias, which is caused by the higher resistivity of W and TiW. As expected, for structure A and C, the via resistance is very stable up to the failure of interconnect while for structure B, the via failed quickly.

Pulse-DC Stressing

Under time-varying current stressing, the electromigration performances can be predicted by using the vacancy relaxation model proposed by Liew et al.[10]. Let δ be the volume of the void caused by the electromigration. The time derivative of δ can be written as:

$$\frac{d\delta}{dt} = R(\delta)n(t)J(t) \qquad (1)$$

where $R(\delta)$ is a proportional constant, which can be a function of δ. n(t) is the vacancy concentration and J(t) is the current density. The time-to-failure, TTF is the time required for δ to reach a critical value δ_c,

$$\int_0^{TTF} n(t)J(t)dt = \int_0^{\delta_c} \frac{d\delta}{R(\delta)} \equiv K \qquad (2)$$

TTF can be defined as the median-time-to-failure(MTTF) or any other failure time. δ_c can be the void volume that causes open failure. According to the vacancy relaxation model, the rate of change for n(t) is the sum of vacancy recombination rate and vacancy generation rate,

$$\frac{dn}{dt} = -\frac{n}{\tau} + \alpha|J(t)|^{m-1} \qquad (3)$$

where τ is the characteristic time constant which affects both the vacancy build-up and decay process, α is a proportional constant. Theoretically, for any given waveform J(t), one can solve Eq.(3) for n(t) and substitute n(t) into Eq.(2) to get TTF.

In order to solve Eq.(3) analytically, a special case of rectangular unidirectional current waveform, i.e., rectangular pulse DC waveform of J(t) is considered for simplicity.

The vacancy concentration n(t) can be obtained by solving Eq.(3) and realizing that the integration of the left hand side of Eq.(3) over one period is zero(under steady state condition), we find the relationship of $MTTF_{pulse-DC}$ and $MTTF_{DC}$ can be written as,

$$MTTF_{pulse-DC} = \frac{MTTF_{DC}}{D\left[1 - \frac{(1 - e^{-aD})(1 - e^{-a(1-D)})}{aD(1 - e^{-a})}\right]} \quad (4)$$

where D is the duty factor, $a \equiv 1/(f\tau)$, f is the pulse DC repetition frequency. From Eq.(4), we can see that in the lower frequency region (i.e., $f << 1/\tau$, $a \rightarrow \infty$),

$$MTTF_{pulse-DC} = \frac{MTTF_{DC}}{D} \quad (5)$$

while in the higher frequency region (i.e., $f >> 1/\tau$, $a \rightarrow 0$),

$$MTTF_{pulse-DC} = \frac{MTTF_{DC}}{D^2} \quad (6)$$

The frequency dependence of $MTTF_{pulse-DC}/MTTF_{DC}$ at peak current density $4.5\times10^7 A/cm^2$ and a duty factor of 50% rectangular waveform for W-plug vias(structure B) is shown in Fig.8. By using Eq.(4), $MTTF_{pulse-DC}/MTTF_{DC}$ is calculated and also shown in Fig.8. We have used τ=0.667ms in the calculation to fit the experimental data. The actual value of τ is a function of temperature, material properties, and grain size, etc.. The via temperature was calibrated by measuring the via resistance, and used to normalize the MTTF to 250°C using a measured activation energy of 0.57eV for our Al-Cu(4wt%) interconnection lines. We can see that the experimental data is in agreement with the model. The discrepancy at high frequency is believed to be due to the error induced in the calibration(e.g., activation energy E_a). Fig.9 and Fig.10 show the calculated results of $MTTF_{pulse-DC}/MTTF_{DC}$ as a function of either frequency or duty factor while holding one variable fixed by using Eq.(4). We can see that the pulse DC lifetime enhancement varies more rapidly with duty factor at high frequencies.

Bidirectional AC Stressing

The via resistances as a function of stressing time under AC, i.e. bipolar stressing conditions are shown in Fig.11. In AC electromigration testing, a current density of 4.5×10^7 A/cm^2 and symmetrical (i.e. 50% duty factor) rectangular bipolar current waveform with zero average current and 1MHz frequency has been used, as shown in Fig.12. We found no open failure and no change in via resistance after stressing for 350 hours for all three via systems. This means that the bipolar lifetime is at least 300 to 1500 times longer than the DC lifetime under the same peak stressing current density. The longer MTTF can be attributed to the healing effect of the two opposite flows of vacancy flux as predicted in [10]. It is proposed that most of the damage incurred during one half-cycle is "repaired" during the opposite half-cycle. This is apparently a general concept that can be applied to vias as well as to interconnects.

Conclusion

Using Kelvin test structures, electromigration characteristics of tungsten and aluminum vias under DC, pulse-DC and bipolar current stressing conditions have been investigated. We find that the lifetimes of Al vias are not only longer than that of W-plug vias, but also longer than the lifetimes of interconnects even though the current density passing through vias is more than 10X larger than the current density passing the interconnects. The low lifetime of Al/W contact vias suggests Al/W contacts present the worst flux divergence locations for electromigration. The addition of TiW layers next to the W-plug can change the electromigration failure mode and improve its electromigration reliability. We also find that the bipolar lifetimes of the test structures are at least two or three orders of magnitude longer than their DC lifetimes. Finally, for pulse-DC via electromigration stressing, we find that the ratio of $MTTF_{pulse-DC}/MTTF_{DC}$ at low frequency region (<200Hz) is about 2, and at high frequency region (>10KHz) is about 4-5. The failure rate as a function of repetition frequency agrees with the behavior predicted by the vacancy relaxation model.

Acknowledgment

The research is supported by SRC and ISTO/SDIO administered by ONR under contract N00014-85-K-0603.

References

[1] V.V. Lee, S.Verdonckt-Vandebroek and S.S. Wong, "A selective CVD tungsten local interconnect technology," in IEDM Tec. Dig., 1988, pp.450-453.

[2] T. Tsutsumi, H. Kotani, J. Komori, and S. Nagao, "A selective LPCVD tungsten process using silane reduction for VLSI applications," IEEE Trans. Electron Devices, vol.37, no.3, pp.569-576, 1990.

[3] R. Mukai, N. Sasaki and M. Nakano, "High-aspect-ratio via-hole filling with aluminum melting by excimer laser irradiation for multilevel interconnection," IEEE Electron Device Letters, vol.EDL-8, no.2, pp.76-78, 1987.

[4] F.S. Chen, Y.S. Lin, G.A. Dixit, R. Sundaresan, C.C. Wei and F.T. Liou, "Planarized aluminum metallization for sub-0.5um CMOS technology," in IEDM Tec. Dig., 1990, pp.51-54.

[5] R.N. Hall, D.M. Brown, R.H. Wilson and D.W. Skelly, "Electromigration reliability studies of intermetal contacts having CVD tungsten via plugs," in Proc. Tungsten and Other Refractory Metals for VLSI Applications III, V.A. Wells, Ed. Pittsburgh, PA: Materials Research Society, 1987, pp.231-237.

[6] F. Matsuoka, H. Iwai, K. Hama, H.Itoh, R. Nakata, T. Nakakubo, K. Maeguchi and K. Kanzaki, "Electromigration reliability for tungsten-filled via hole structure," IEEE Trans. Electron Devices, vol.37, no.3, 1990, pp.562-567.

[7] J.J. Estabil, H.S. Rathore and F. Dorleans, "The effect of metal thickness on electromigration induced extrusion shorts in submicron technology," in Proc. 1991 International Reliability Physics Symposium, 1991, pp.57-63.

[8] J.S. May, "Electromigration characteristics of vias in Ti:W/Al-Cu(2wt%) multilayered metallization," in Proc. 1991 International Reliability Physics Symposium, 1991, pp.91-96.

[9] J.A. Maiz, "Characteristics of electromigration under bidirectional(BC) and pulsed unidirectional(PDC) currents," in Proc. of 1990 International Reliability Physics Symposium, 1990, pp.220-228.

[10] B.K. Liew, N.W. Cheung and C. Hu, "Projecting interconnect electromigration lifetime for arbitrary current waveforms," IEEE Trans. Electron Devices, vol.37, no.5, pp.1343-1351, 1990.

[11] Jiang Tao, K.K. Young, C.A. Pico, N.W. Cheung and C. Hu, "Electromigration characteristics of tungsten plug vias under pulse and bidirectional current stressing," IEEE, Electron Device Letters, vol.12, no.12, pp.646-678, 1991.

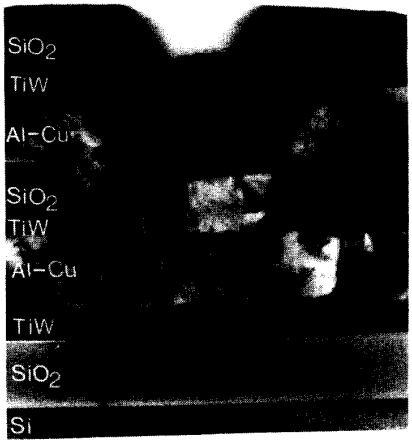
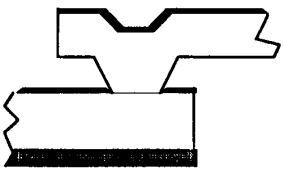
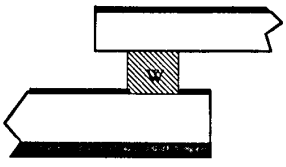
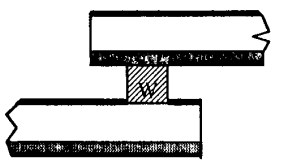


Fig.1 TEM(cross-section) micrograph of structure A(Al-via).

(a) (b)

Fig.2 SEM micrographies shown the open failure of structure A(Al via) under J_{DC} = 3.5×10^7A/cm^2 and T=250°C for electron flow from M1 to M2(a) and M2 to M1(b). No via failure was observed because the interconnect failed first.

Table I. Electromigration failure results of different test structures under $J_{DC} = 3.5\times10^7$ A/cm^2, T=250°C.

Test Structures	Electron Flow Direction M1 to M2	Electron Flow Direction M2 to M1
Structure A 	No failure at vias All opened at interconnects (Total 9 samples were tested)	No failure at vias All opened at interconnects (Total 9 samples were tested)
Structure B 	All opened at vias MTTF = 0.7 hours No open failure at interconnect (Total 9 samples were tested)	Three opened at vias MTTF = 1.3 hours Six opened at interconnects (Total 9 samples were tested)
Structure C 	No failure at vias All opened at interconnects (Total 8 samples were tested)	All opened at vias MTTF = 0.2 hours No open failure at interconnect (Total 8 samples were tested)

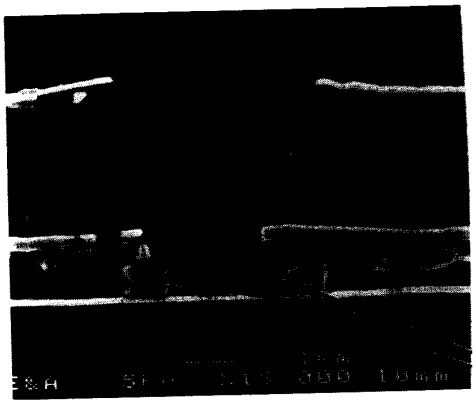


Fig.3 SEM (cross-section) micrograph shows the failure of structure B(W-plug) under $J_{DC}=3.5\times10^7 A/cm^2$ and T=250°C for eleectron flow from M2 to M1.

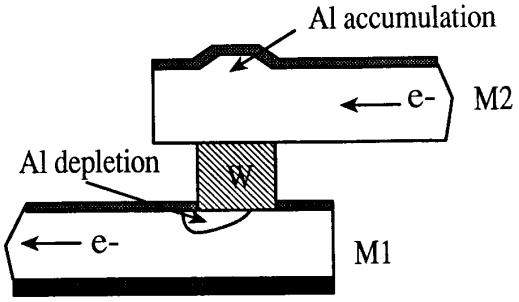


Fig.4 The aluminum accumulation and depletion at the top and bottom of W-plug via area when electron flow was from M2 to M1 for structure B(W-plug).

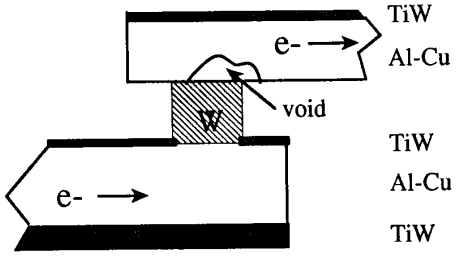


Fig.5 The void formation at via contact area when electron flow was from M1 to M2 for structure B(W-plug).

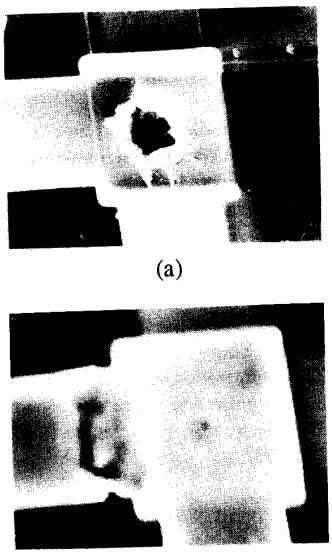


Fig.6 SEM micrographs of (a)structure B and (b) structure C after open failure was created by electron flow from M1 to M2 under $J_{DC}=3.5\times10^7 A/cm^2$, T=250°C.

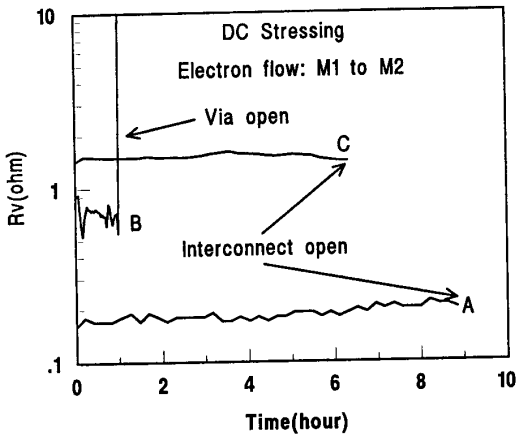


Fig.7 Via resistances versus stressing time under $J_{DC}=3.5\times10^7 A/cm^2$ and T=250°C with electron flow from M1 to M2.

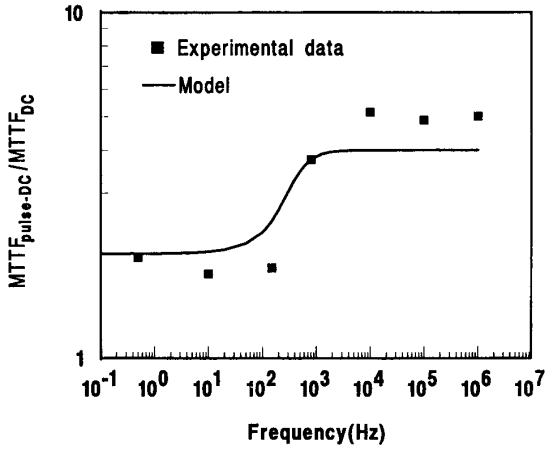


Fig.8 Normalized pulse DC lifetime $MTTF_{pulsed-DC}/MTTF_{DC}$ as a function of current repetition frequency for structure B. The test structure was stressed at J_{DC} = $4.5\times10^7 A/cm^2$ and T=250°C for electron flow from M1 to M2.

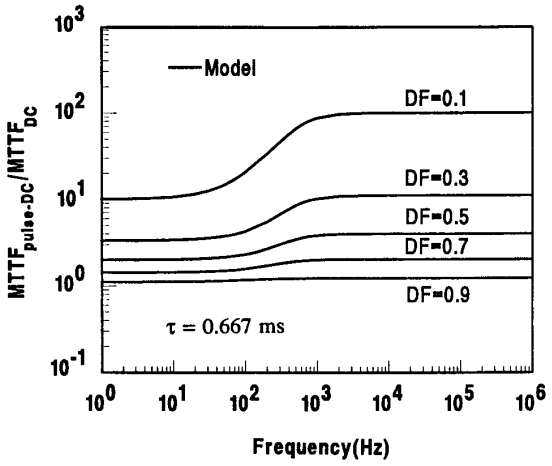


Fig.9 The calculated results of $MTTF_{pulse-DC}/MTTF_{DC}$ as a function of pulse repetition frequency for different duty factors by using the vacancy relaxation model.

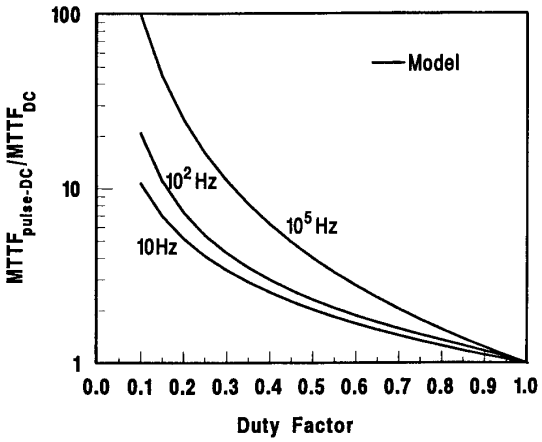


Fig.10 The calculated results of $MTTF_{pulse-DC}/MTTF_{DC}$ as a function of pulse duty factor for different frequencies by using the vacancy relaxation model.

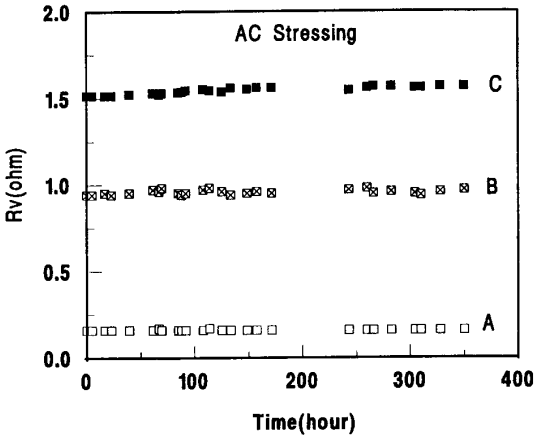


Fig.11 Via resistances versus stressing time under bidirectional current stress. 1MHz rectangular current waveform has peak to zero current density of J_{AC} = $4.5\times10^7 A/cm^2$, i.e. peak to peak at $9\times10^7 A/cm^2$. The substrate temperature is T=250°C.

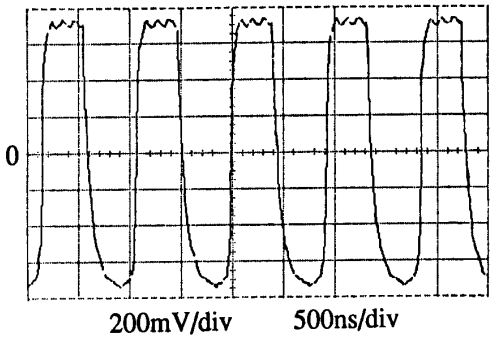


Fig.12 The bidirectional current waveform used in the AC electromigration stressing.