I/O DEVICE DRAIN ENGINEERING FOR A 5V 0.6um CMOS TECHNOLOGY

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ABSTRACT

The ESD robustness of LATID (Large Angle Tilted Implanted Drain) MOSFET for I/O drivers is evaluated and found inadequate for deep sub-micron 5V CMOS technology. Alternative drain structures are examined and reported to meet the ESD and other criteria. An additional phosphorous implant that creates a LATID/DDD (Double Diffused Drain) structure meets all ESD and device criteria.

I. INTRODUCTION

LDD (Lightly Doped Drain) has been a common N-channel MOSFET structure to meet hot electron lifetime criteria for near and sub-micron MOS technology. For deep sub-micron 5V technology, LDD may not be adequate and LATID (Large Angle Tilted Implanted Drain) is adopted to further improve, and meet stringent hot carrier life time criteria [1]. However, for the I/O buffer ESD immunity is equally important. While many devices and protection schemes can be used for input circuits, output and I/O circuits need to be self protected because the drain of the MOSFET is directly tied to the pad. Low ESD failure threshold has been reported on the LDD drain structure of output and I/O circuits. Alternative approaches such as DDD (Double Diffused Drain) and MDD (Moderately Doped Drain) are necessary to meet ESD criteria. Good results of such application to LDD technology on I/O have been reported [2,3]. However, ESD immunity of LATID device has not been reported yet. The effectiveness of the DDD application in conjunction with the LATID device needs to be reexamined also. We found that the phosphorous DDD implant lateral profile can not overwhelm LATID implant profile. This is because of both the longer tail of the drain lateral doping profile from the large angle implant and the low-thermal-budget of the 0.6um technology. The diffusion temperature is low in order to obtain shallow junctions and to suppress the short channel effects. This paper reports the ESD failure threshold and other relevant device data of LATID device, together with DDD device and MDD device as alternative implementations for the I/O buffer.

II. EXPERIMENTS

A twin well, tungsten-silicided-gate, 135A gate oxide, double metal, 0.6um process is used to fabricate four types of drain structure, namely LATID, "LATID+DDD" device, DDD and Large Angle Tilted Implanted MDD (LAMDD). The large angle tilted implant is done by a Varian E220 ion planer. For LDD implant, the angle is set at 30 degree. For MDD implant, the angle is varying from 0, 30 to 60 degree. The DDD implant is done at 7 degree.

The resulting source/drain lateral doping profile is illustrated in figure 1. Among the four types of device, "LATID+DDD" is actually a hybrid of LDD and DDD (figure 1.3). LAMDD is further studied on varying implant angle and energy to create different doping concentration and junction depth. The process flow is as follows:
Figure 1. Cross section of four device structures studied in this work.

Figure 2. Schematics of I/O buffers.

... Front-end process
- Silicided gate formation
- Phosphorous LATID, LAMDD or none (split)
- PLDD implant
- Spacer formation
- N+ source/drain
- Phosphorous DDD or none (split)
- Implant anneal
- P+ source/drain

... Back-end process ...
The process splits are as follows:

Device type  LATID/MDD implant  DDD implant

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<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>1. LATID</td>
<td>2.4E13 30°</td>
<td>no implant</td>
</tr>
<tr>
<td>2. DDD</td>
<td>no implant</td>
<td>4E15 7°</td>
</tr>
<tr>
<td>3. LATID+DDD</td>
<td>2.4E13 30°</td>
<td>4E15 7°</td>
</tr>
<tr>
<td>4. MDD</td>
<td>5E13 0° 80keV</td>
<td>no implant</td>
</tr>
<tr>
<td>5. LATI-MDD</td>
<td>5E13 30° 70keV</td>
<td>no implant</td>
</tr>
<tr>
<td>6. LATI-MDD</td>
<td>5E13 30° 90keV</td>
<td>no implant</td>
</tr>
<tr>
<td>7. LATI-MDD</td>
<td>5E13 60° 70keV</td>
<td>no implant</td>
</tr>
<tr>
<td>8. LATI-MDD</td>
<td>5E13 60° 90keV</td>
<td>no implant</td>
</tr>
</tbody>
</table>

III. RESULTS AND DISCUSSIONS

A dedicated 0.6um ASIC test vehicle is used for I/O evaluation. This test vehicle contains various types of CMOS I/O cells for advanced cell library and gate array products. It includes a variety of input, output and I/O cells. The layout of these cells are the same below the metal levels. Metal masks are used to create different I/O cells. For an input cell, The large output transistors are shut off and become protection devices (Figure 2a).

The experimental results are summarized in the following paragraphs:

1. ESD failure threshold (ESD robustness)

ESD zap test was done with Human Body Model (HBM). Because this test vehicle has very little core circuits, we have found the HBM failure threshold is lower than a real product which contains a sizable core. So the reported data is the worst case for our ASIC devices. Figure 3 shows the ESD failure threshold distributions of LATID and "LATID+DDD" devices. The ESD robustness of LATID is lower (similar to the LDD device), and fails the 2,000V MIL class II ESD specification. However, this specification can be met by adding DDD implant to the I/O device. Figure 4 shows the failure threshold of all the splits. DDD offers the best ESD robustness, unfortunately it has poor hot electron lifetime.

![Figure 3. HBM ESD failure threshold distribution.](image3)

![Figure 4. ESD failure threshold of various device structures.](image4)

![Figure 5. Effective channel length (L_eff) vs. gate length of mask (L_m)].
2. Effective channel length and threshold voltage roll-off

Because of different drain structure, the lateral encroachment of all devices are different. Figure 5 shows the effective channel length (Leff) for a range of mask channel length (Lm). For the DDD structure, Leff is almost identical to Lm, indicating the DDD implant after spacer barely reaches to the edge of the polycide gate. The Leff of LATID is almost the same as that of "LATID +DDD" device. This data indicate that LATID implant dominates the lateral encroachment underneath the gate and the DDD implant stops short of the edge of the LATID implant (as illustrated in figure 1c). Vt roll-off is a good figure of merit for the short channel effect. Figure 6 shows the Vt roll-off characteristics of all splits. They show similar characteristics.


Saturation current is the major figure of merit for the speed performance of a digital circuits. Figure 7 shows the saturation current (measured at Vds = Vgs = 5V, W = 20um) versus Leff. It is best to compare Idsat at minimum allowable Leff. Table 1 lists the corresponding gate length, channel length and Idsat for a specific Vt roll-off of 250mV. We find "LATID+DDD" device provides the highest Idsat, while LATID device has lowest Idsat due to higher source/drain resistance. All device types have similar Leff when Vt rolls off of 250mV. But the Lmask is different due to different lateral encroachment.

4. Hot carrier lifetime

Hot carrier lifetime is the major figure of merit for device reliability. Figure 8 shows
Table 1. Short channel effect and Idsat comparison. These Lmask and Leff meet the criteria of 0.25V Vt roll off at Vds = 5V.

<table>
<thead>
<tr>
<th>Device type</th>
<th>LATID</th>
<th>DDD</th>
<th>LATID+DDD</th>
<th>MDD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lmask (um)</td>
<td>0.55</td>
<td>0.51</td>
<td>0.58</td>
<td>0.63</td>
</tr>
<tr>
<td>Leff (um)</td>
<td>0.45</td>
<td>0.45</td>
<td>0.48</td>
<td>0.47</td>
</tr>
<tr>
<td>Idsat (uA/um)</td>
<td>505</td>
<td>525</td>
<td>557</td>
<td>535</td>
</tr>
</tbody>
</table>

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<thead>
<tr>
<th>LAMDD</th>
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</tr>
</thead>
<tbody>
<tr>
<td>30°</td>
<td>30°</td>
<td>60°</td>
<td>60°</td>
</tr>
<tr>
<td>70keV</td>
<td>90keV</td>
<td>90keV</td>
<td>90keV</td>
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</tbody>
</table>

Figure 8. DC hot electron lifetime vs. gate length (100mV threshold voltage shift).

The hot carrier lifetime data measured by accelerated stress measurement. LATID device is the best among all device types. "LATID+DDD" device has superior hot electron lifetime than LATI-MDD and DDD structure. This is expected because a lightly doped N-region exists to relax drain electrical field.

The combination of excellent ESD robustness, Idsat and hot carrier lifetime make "LATID+DDD" a best choice in all the experimental devices.

IV. CONCLUSION

In conclusion, LATID device, similar to LDD device, provides good hot carrier lifetime but poor ESD robustness. DDD device however, provides good ESD robustness but poor hot carrier lifetime. A hybrid "LATID+DDD" is ideal for I/O buffer because it provides sufficient ESD immunity and reasonable hot carrier lifetime with minimum over-size of gate length. LAMDD also provides improvement on ESD over LATID but not as much as "LATID+DDD" device.

REFERENCE

