**Nearly-Fully-Depleted (NFD), 0.15μm SOI CMOS in a CBICMOS Technology**

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**Abstract**
Complementary 0.15μm MOSFETs and double-diffused lateral BJT's have been successfully integrated in a 10-mask CBICMOS process, by utilizing the process simplifications that are unique to thin-film SOI. The CMOS devices are built in a SIMOX silicon layer of intermediate thickness (130nm), leading to Nearly-Fully-Depleted (NFD) characteristics. Excellent short-channel behavior is observed down to $L_{eff}=0.15μm$. P+ gate, NFD-SOI PMOSFETs with $t_{ox}=5.5nm$ exhibit record high performance, with $f_{sat}=274mS/mm$ and $352mS/mm$ at 300K and 80K, respectively. Propagation delays of 25ps/stage and 17ps/stage were measured on unloaded CMOS and NMOS ring oscillators, respectively, at $V_{dd}=3.3V$ and room temperature.

**Introduction**
Over the past few years, much focus has been given to fully-depleted SOI MOSFETs, due to improved subthreshold slope, suppression of the floating-body effects, and higher mobility as compared with partially-depleted SOI devices. Several Ultra-Thin-Film (UTF), fully-depleted SOI device designs have been reported [1-6]. In some cases, reductions in punchthrough and short channel effects have been mistakenly assumed to be further attributes of full-depletion. In fact, these improvements are the result of the thinness of the SOI film and/or higher channel doping, which may also be achieved in a Nearly-Fully-Depleted (NFD) device. Also, many of these reported fully-depleted devices suffer from high series resistance as the result of a small source/drain cross-sectional area. Implementing a titanium salicide process on UTF-SOI is more difficult than on bulk, and leads to non-ohmic contact behavior in some cases [7].

It is also difficult to achieve a large enough threshold voltage in a fully-depleted device, without using a mid-gap gate workfunction. The fully-depleted threshold voltage is very sensitive to variations in the SOI film thickness. For deep-sub-micron SOI devices, body doping in the range of $5x10^{17/cm^3}$ will be required to control punchthrough, DIBL, and short channel effects. As seen in Fig. 1, the threshold voltage sensitivity to SOI film thickness variations is very high in this doping range ($\Delta V_t=0.2V$ for $\Delta t_{soi}=10nm$).

![Threshold voltage vs. SOI film thickness](image)

**Fig. 1** Threshold voltage vs. SOI film thickness. $V_t$ is independent of $t_{soi}$ for partially-depleted devices. $V_t$ is a linear function of $t_{soi}$ for fully-depleted devices, with increasing sensitivity at higher body doping.

This paper describes Nearly-Fully-Depleted (NFD) SOI CMOS devices with $t_{soi}=130nm$ and $N=1x10^{17/cm^3}$, resulting in a threshold design near the boundary of full-depletion. In saturation ($V_d=2.5V$), only a small region of the body near the source remains un-depleted.
A significant portion of the channel has reduced vertical field, increased mobility, and increased inversion charge, as in a fully-depleted device, due to the constrained bulk charge. However, the device threshold voltage is insensitive to SOI thickness variations, as in a partially-depleted device, as long as a small quasi-neutral body region remains near the source. Reasonable series resistance values of 700 $\Omega \mu m$ and 1100 $\Omega \mu m$ for the NMOS and PMOS, respectively, were achieved, even without the use of SAlicide, due to the larger film thickness and a high S/D implant dose.

**Device Processing**

SIMOX substrates were supplied by IBIS Corp. Device isolation was performed by the ReOxidized Silicon Island Edges (ROSIE) isolation technique, in which the isolation pad is used as an etch mask to create SOI silicon islands. The pad is left in place, and the exposed island edges are reoxidized in a wet oxygen ambient. The 100nm oxide grown on the sidewalls of the SOI islands has two positive results. First, gate oxide thinning is prevented at the silicon island corners. Second, sub-threshold leakage current along the NMOS device edges is reduced significantly, as compared with SOI NMOS devices using LOCOS isolation. This is because the ROSIE process leaves no thin silicon regions at the device edges. Both 5.5 and 10nm gate oxides were grown, followed by the deposition of 280nm of undoped polysilicon. The poly gates and source/drain regions were doped by $10^{16}$/cm$^2$ boron and arsenic implants, resulting in p+ gate PMOS and n+ gate NMOS surface-channel devices. Effective channel lengths as short as 0.08$\mu m$ were obtained by oxygen plasma "ashing" of the gate photoresist, prior to the gate etch.

**Device Performance**

Fig. 2 shows the $I_d$-$V_d$ characteristics for 0.18$\mu m$ NMOS and PMOS devices with $t_{ox}$=10nm. The saturated drain current per micron of width is 0.7mA for the NMOS and 0.33mA for the PMOS, at $V_{gt}$=$V_d$=2.5V. These results are superior to the previously cited works [1-6]. A small floating-body "kink" is observed in both device characteristics for $V_{gt}$<1.0V. At higher gate voltage, this kink voltage merges with $V_{dsat}$.

Long-channel threshold voltages of +0.83V and -0.48V were obtained for the NMOS and PMOS devices, respectively. The sub-threshold characteristics for the short-channel devices of Fig. 2 are shown in Fig. 3, with $S$=80mV/decade for both. The NMOS

![Fig. 2](image-url)
characteristic exhibits some additional sub-$V_T$ leakage current along the device edges, even with ROSIE isolation. This is due to boron segregation out of the SOI island sidewalls, and may be suppressed by doping the NMOS device edges, or the entire channel, more heavily. Excellent short channel behavior is observed for these devices, as shown in Fig. 4. Both $\Delta V_T$ and subthreshold swing show almost no change down to $L_{eff}=0.2\mu m$. This behavior is equivalent to that of much thinner UTF-SOI films.

The peak saturation transconductance is shown in Fig. 5, as a function of channel length. PMOS devices with $L_{eff}=0.08\mu m$ exhibit $g_{msat}=160 mS/mm$, while NMOS devices with $L_{eff}=0.13\mu m$ have $g_{msat}=240 mS/mm$.

P+ gate, NFD-SOI PMOSFETs with a scaled gate oxide thickness of 5.5nm exhibit $g_{msat}=274 mS/mm$ at 300K and 352 mS/mm at 80K, as shown in Fig. 6. A remarkable peak current drive of 0.55mA/$\mu m$ was found at 80K. This performance is higher than any other reported SOI or bulk PMOSFETs at this gate oxide thickness and channel length.

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Fig. 7 shows the excellent short-channel behavior of the PMOSFETs as compared with a recent state-of-the-art bulk PMOS design. The ability to make very high-performance, shallow-junction, short-channel PMOSFETs may be the strongest motivation to migrate from bulk to SOI for sub-0.25μm CMOS.

Circuit Performance

101-stage, unloaded CMOS inverter ring oscillators have been fabricated in this technology, with Wp/Wn=10μm/5μm. The NMOS L_eff=0.33μm, while the PMOS L_eff=0.08μm. The 0.25μm difference in L_eff is due to the large lateral diffusion of the boron source/drain junctions. The ring oscillators exhibit a propagation delay of 25ps/stage at VDD=3.3V and 300K [8]. At VDD=5V, the delay is reduced to 17ps/stage, as shown in Fig. 8.

These CMOS circuit performance results are superior to SOI CMOS circuits previously reported [10-12]. Depletion-mode NMOS ring oscillators fabricated in this technology have demonstrated the shortest propagation delay (13.5ps/stage) for any silicon circuit (bipolar or MOSFET) reported to date [9].
References