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Impact of Polysilicon Depletion in Thin Oxide MOS Technology

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Abstract

Accurate characterization of thin oxide conduction current, breakdown, and MOSFET current require an accounting for the voltage drop due to the depletion of the polysilicon gate. The reduction of oxide thickness and polysilicon doping ascerbate this effect. Scaled n+/p+ dual gate CMOS technology incorporates both these trends, due to process integration constraints which limit the concentration of active dopants in polysilicon. This paper investigates effects of polysilicon depletion on the thin oxide MOS system.

Polysilicon Gate Depletion: Determination of Band Bending in Polysilicon

In thicker oxides, the gate (GE) and substrate emission (SE) tunneling characteristics tend to be parallel, with an offset due to band bending [1]. Fig. 1 shows that the measured IV characteristics in very thin oxides are not parallel. This is a result of the polysilicon depletion. Fowler-Nordheim tunneling current shold be a unique function of the oxide voltage, independent of polarity. Computation of the oxide voltage for each curve by subtracting for band bending in the poly-gate and the substrate reduces them to a single tunneling characteristic dependent only on V_{ox}. The polysilicon band bending induces

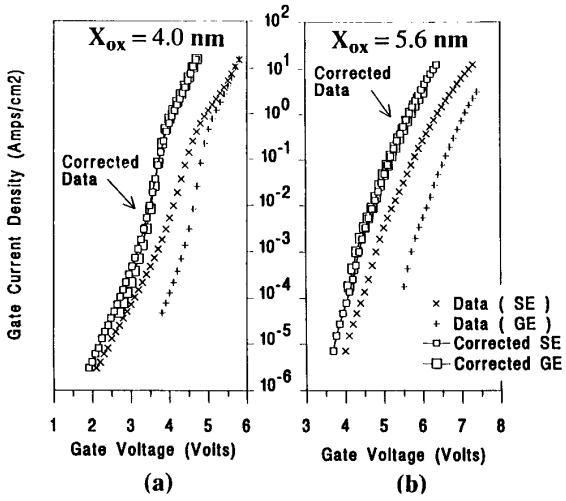

Fig. 1 J-V characteristics for a) 4.0 nm and b) 5.6 nm oxide capacitors. The corrected data for substrate emission (SE) is computed by subtracting the voltage drop due to polysilicon band bending with N_{poly} = 5.0 x 10^{19} cm^{-3}. Gate Emission (GE) is corrected with a parallel voltage shift of about 1.2 V. Decreasing thickness enhances magnitude of polysilicon depletion.

a voltage drop correcting the GE and SE curves under the transformations

$$\text{GE: } V_{ox} = E_{ox}X_{ox} = V_g - 1.1 \quad (1)$$

$$\text{SE: } V_{ox} = E_{ox}X_{ox} = \left(V_g - 0.2\right) - V_{poly} \quad (2)$$

$$V_{poly} = \frac{\varepsilon_{ox}^2 E_{ox}^2}{2q\varepsilon_{Si}N_{poly}} \quad (3)$$

until V_{poly} is pinned at 1.12 V due to the saturation of band

bending in strong inversion, a situation not likely to be encountered in practical heavily doped polysilicon.

Determination of Active Impurity Concentration

Test capacitors have been fabricated on n-Si to provide deliberately lightly-doped n-type polysilicon gate electrodes with varying phosphorus implant dose. Poly and gate oxide thicknesses are 2800 Å and 68 Å, respectively. Samples were implanted at 20 keV and subsequently furnace annealed in N_2 ambient for 20 minutes at 900 C. The 4 kHz Capacitance-Voltage characteristic in Fig. 2 shows that the observed capacitance degradation from C_{ox} increases with decreasing doping according to a larger poly depletion capacitance (in series with the gate oxide capacitance). Moreover, the onset of recovery, i.e. the gate voltage at which the hole inversion layer begins to form in the poly-Si, increases with the doping

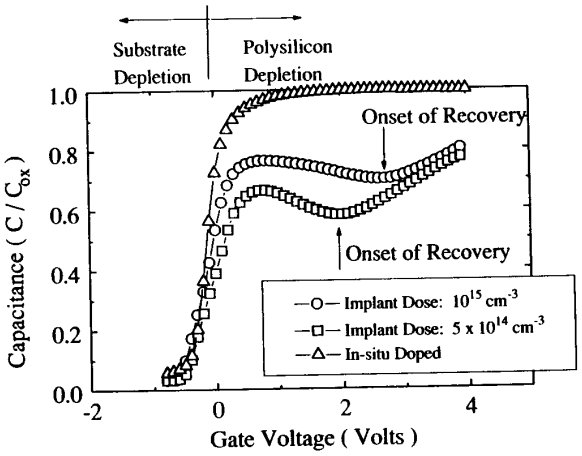

Fig. 2 Capacitance-Voltage (CV) measurement of lightly-doped polysilicon MOS capacitors at 4 kHz. Capacitance does not reach C_{ox} due to the series effect of the depletion capacitance in the polysilicon. Recovery indicates the formation of a hole inversion layer which screens the depletion charge, so that the series capacitance increases.

concentration, consistent with the expected suppression of the depletion effect for higher polysilicon doping concentration.

Fig. 3 shows the estimation of Electrically Active Impurity Concentration of the implanted samples using the voltage correction technique demonstrated in Fig. 1. The GE curves are coincident, regardless of poly doping, whilst the SE curves show varying amounts of shift according to the electrically active impurity concentration. We interpret this concentration as the dopant concentration in the bulk of the polysilicon grains. The weak dependence of active concentration on implant dose (Fig. 4) indicates that most of the implanted dopants reside at inactive sites at grain boundaries. Fig. 5 compares the expected bulk resistivities corresponding to these active doping concentrations with measured poly resistivities. At lower implant dose, the bulk resistivity corresponding to the active impurity concentration is much lower than observed, implying that the high resistivity is due to the resistance of the grain boundary, which has been modeled by thermionic emission [2]. At higher implant doses, the polysilicon resistivity drops significantly because of increased dopant density at the grain boundaries although the dopant concentration in the bulk of the grains (Fig. 4) increases only slightly. At very high dopant concentrations, e.g. an in-situ doped sample, the polysilicon resistivity approaches that of the bulk resistivity expected from the extracted active dopant concentration. Comparison with in-situ phosphorus doped poly suggests that 5 x 10^{19} cm^{-3} poses a practical upper limit to the electrically active impurity concentration.

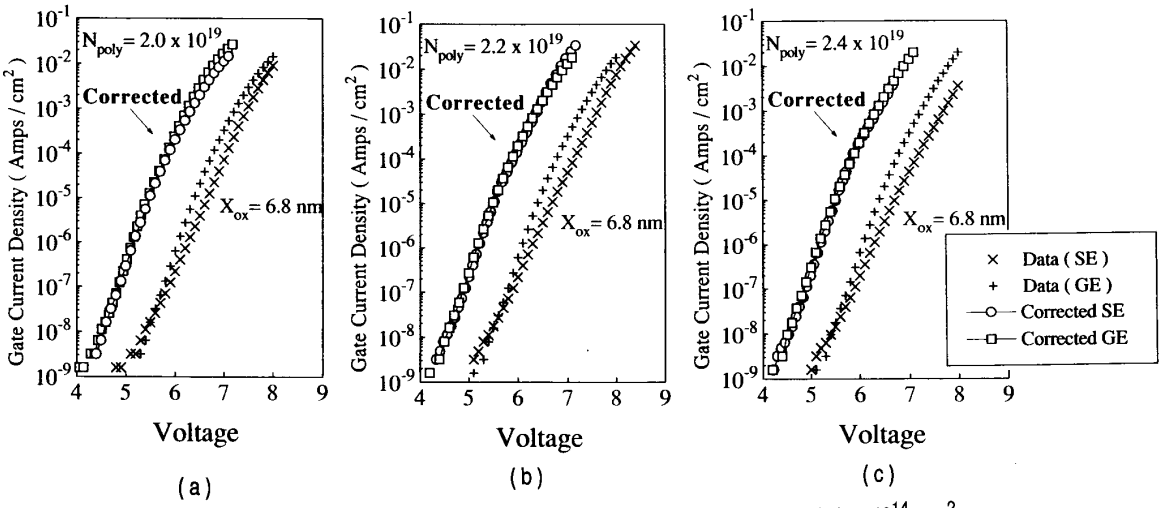

Fig. 3 J-V characteristics for lightly-doped polysilicon 6.8 nm oxide capacitors. Implant dose: (a) 2 x 10^{14} cm^{-2} (b) 5 x 10^{14} cm^{-2} (c) 10^{15} cm^{-2}. Correction for polysilicon depletion effect extracts effective Electrically Active Impurity Concentration: (a) 2 x 10^{19} cm^{-3} (b) 2.2 x 10^{19} cm^{-3} (c) 2.4 x 10^{19} cm^{-3}.

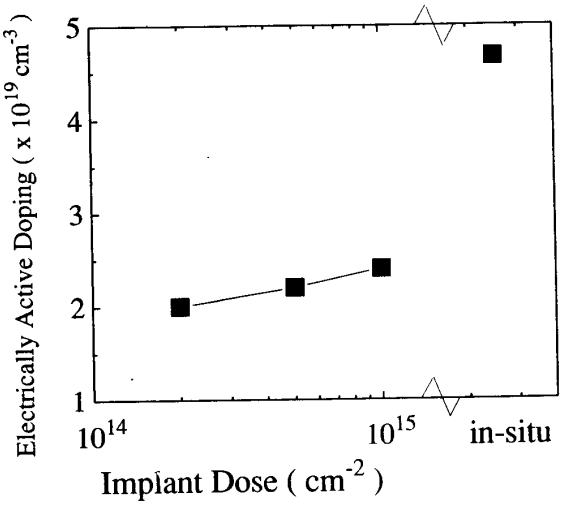

Fig. 4 Electrically Active Impurity Concentration as function of ion implant dose, compared with that of in-situ doped polysilicon. Most of the implanted dopants appear to be residing at electrically inactive sites at the grain boundary.

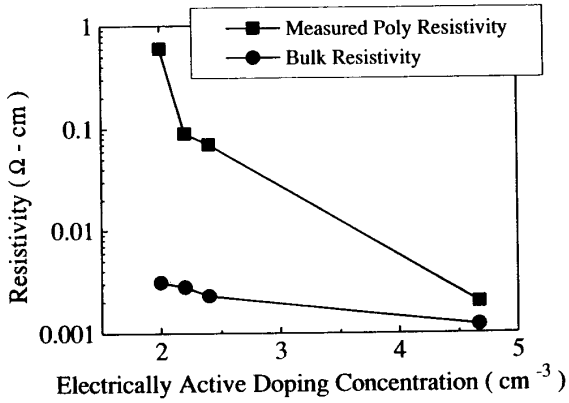

Fig. 5 "Tabulated" resistivities of bulk silicon corresponding to the effective Electrically Active Impurity Concentration compared with the measured resistivities of polysilicon. Implies the grain boundaries determine resistivity.

Implication of Polysilicon Depletion on Device Performance

Since process integration issues for n+/p+ dual-gate technologies will dictate achievable dopant activation [3], we investigate the impact of reduced dopant activation on available transistor drive current and on supply voltage scaling. The channel inversion charge (proportional to transistor linear-region current) is simply $C_{ox}(V_g - V_T)$, absent of depletion, and $C_{ox}(V_g - V_{poly} - V_T)$ in the presence of depletion. The ratio $(V_g - V_{poly} - V_T)/(V_g - V_T)$ measures the "efficiency" of a depletion-degraded transistor. Fig. 6 illustrates the thickness variation of this quantity as a function of supply voltage and polysilicon active doping. Depletion caused degradations are

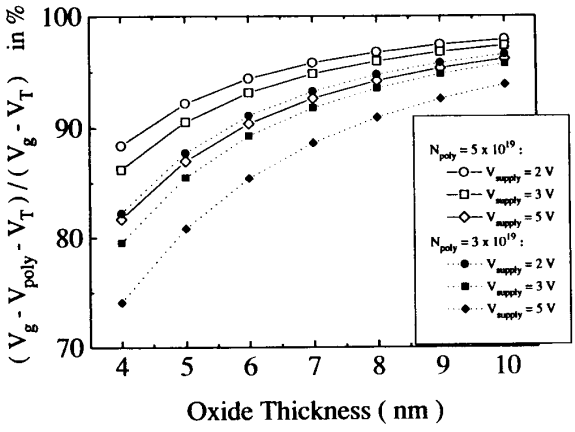

Fig. 6 Thickness Dependence of (V_g - V_{poly} - V_T) / (V_g - V_T) which measures the efficiency of a transistor degraded by polysilicon depletion. Lower active polysilicon doping, thinner oxides, and higher voltages enhance polysilicon depletion-caused degradation. This applies to n+-gate NMOSFET and p+-gate PMOSFET.

worse for lower polysilicon dopings and thinner oxides and better for lower voltages. It may seem surprising that the performance reduction due to depletion for devices with the large electrically active dopant concentration of 5 x 10^{19} cm^{-3} operated at 5 V is the same as that of 3 X 10^{19} at 2.5 V. This is true if the two devices have the same oxide thickness. In reality, the low voltage device will almost certainly have a thinner oxide. If we consider constant oxide field or constant V_g / X_{ox}, reduction of V_g worsens the polysilicon depletion effect. In contrast, n+-gate PMOSFET (and p+-gate NMOSFET) does not suffer from this effect.

Polysilicon gate depletion is not expected to have an impact on the gate-induced drain leakage (GIDL), i.e. band-to-band tunneling leakage current [4], on n+-gate NMOS and p+-gate PMOS transistors, since the oxide field polarity corresponds to polysilicon accumulation. Polysilicon depletion tends to decrease GIDL in comparison to n+-gate PMOSFET without polysilicon depletion. However, even with polysilicon depletion, n+-gate PMOSFET will have larger gate-induced drain leakage than p+-gate PMOSFET because of the gate work function difference [5].

Fig. 7 compares the thickness dependence of maximum acceptable voltage for 10 year intrinsic oxide lifetime [6] for in-situ doped poly, active doping concentration of 2.5 x 10^{19} cm^{-3}, and the depletion free case. The increasing percent

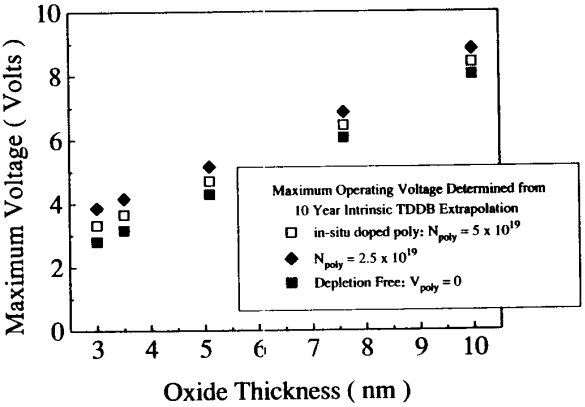

Fig. 7 Time Dependent Dielectric Breakdown (TDDB) poses limits on maximum acceptable supply voltages. More highly doped polysilicon requires derated supply voltages because polysilicon voltage drops are lower.

spread of these voltages, up to 35%, for thinner oxides highlights the necessity of accounting for polysilicon depletion in thin oxide reliability extrapolation.

Acknowledgements

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References

[1] E. Rosenbaum et al. in *Int. Symp. VLSI TSA*, p. 214, 1991.
[2] T. Kamins, Polycrystalline Silicon for IC Applications, Ch. 5, 1988.
[3] C. Lu et al., *IEEE Elec. Dev. Let.*, p. 192, 1989.
[4] H. Wann et al. in *Int. Elec. Dev. Mtng.*, p. 147, 1992.
[5] J. Chen et al., *IEEE Elec. Dev. Let.*, p. 515, 1987.
[6] K.F. Schuegraf et al., *Intl. Rel. Phys. Symp.*, p. 7, 1993.