HOT-CARRIER-RELIABILITY OF MIXED ANALOG/DIGITAL TECHNOLOGIES

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Abstract: DC lifetime, in conjunction with speed and time factors, can be used to predict digital circuit hot-carrier lifetime. Analog circuit reliability prediction, on the other hand, has to take analog design variables such as channel length, biasing conditions, and circuit topography into consideration.

We propose a new methodology for predicting analog circuit reliability. Instead of the traditional lifetime plots, we present a set of analog hot-carrier design curves that span the analog design space. The design curves will become increasingly important for high speed analog applications and for ULSI chips that integrate a wide variety of analog and digital functions. The design curves can be used to quickly estimate the hot-carrier sensitivity of a particular analog sub-block and to adjust the design variables for better hot-carrier immunity.

I. INTRODUCTION

The focus of hot-carrier-reliability has shifted towards the understanding of the relation between DC degradation and circuit degradation [1-4]. With the integration of more and more functions on a single chip, mixed analog and digital technology will drive ULSI chips. While most of the hot-carrier circuit reliability studies have primarily been targeted for digital applications, very limited work has been done on applications requiring analog functions [5-8]. For state-of-the-art technologies, it is sufficient to predict digital circuit hot-carrier reliability based on drain current change of single transistors with minimum $L_{eff}$ of a given process. Since analog circuit design includes several variables, such as, $L_{eff}$, bias conditions, and circuit topography, existing lifetime prediction methodology commonly used for digital circuits are not adequate. Thus an understanding of hot-carrier reliability of analog device parameters and their impact on analog circuits is essential, not only for dedicated analog chips, but for the impact of analog circuit reliability in a digital technology. Two different LDD technologies, one with $L_{eff} = 0.5\mu m$ and $T_{ox} = 17.5nm$ and the other with $L_{eff} = 1\mu m - 6\mu m$ and $T_{ox} = 21nm$, were used in this study. In this paper, we present a set of analog hot-carrier design curves that can be used for design optimization and for lifetime prediction by reliability and circuit designers.

II. DIGITAL CIRCUIT HOT-CARRIER-RELIABILITY

Figure 1 shows the fresh and degraded $I_{ds}$ of an NMOSFET after hot-carrier stressing. There is now a consensus among most research groups that the primary mechanism of digital circuit degradation is interface states and that a quasi-static approach is valid for digital circuit lifetime prediction [3,9,10].

NMOSFET DC device lifetime can be expressed as [11,12],

$$\tau_{d} = \frac{I_{ds}}{I_{subs}} - \frac{m}{H}$$

where $W$ is the device width, $H$ and $m$ are hot-carrier degradation parameters, and $I_{subs}$ and $I_{ds}$ are the substrate and drain currents respectively. The device lifetime, $\tau_{d}$, at some fixed amount of degradation, $\Delta D$, such as 10% change in drain current can, be obtained from figure 2. The hot-carrier induced change in drain current can be translated to digital circuit speed degradation using speed and time factors [2,10].
as shown in figure 3. Digital circuit lifetime can then be predicted using figures 2 and 3. NMOSFET DC lifetime at 10% change in linear drain current is 0.15 years for 5V operation. Figure 3 shows that inverter based digital circuits operating at 58 MHz will change 1.5% in 3.3 years.

III. ANALOG DEVICE PARAMETER DEGRADATION

Figure 1 shows that the degraded \( I_{ds} \) approaches the fresh \( I_{ds} \) with increasing \( V_{ds} \). This is because at low \( V_{ds} \), the interface states are occupied and negatively charged; however, with increasing \( V_{ds} \), they are emptied and become neutral. Thus, in addition to decreasing the drain current, the shape of the poststress I-V characteristic is significantly altered. This is reflected in figure 4 that shows the fresh and degraded output resistance, \( R_{out} \), of a 3µm NMOSFET device. Figure 5 shows the saturation region fresh and degraded \( I_{ds} \) as a function of \( V_{gs} \). Let us now consider the virtual differential pair shown on the left of figure 5. If only transistor \( M_R \) undergoes significant hot-carrier stressing (worst case), then we can represent the \( I_{ds} \) - \( V_{gs} \) characteristics of transistors \( M_L \) and \( M_R \) by the fresh and degraded curves respectively. After hot-carrier stressing, the same drain current in both transistors can only be obtained by increasing \( V_{gs} \) of \( M_R \) by \( \Delta V_{off-set} \). Figure 6 shows a single-
ended output CMOS differential amplifier. Gain and offset voltage are the two most important design parameters for the differential amplifier. The gain, $G$, of the differential amplifier is given by

$$G = \frac{g_{m1}}{(g_{d1} + g_{d2})}$$

(2)

where $g_{m1}$ and $g_{d1}$ are the transconductance and output conductance of the NMOSFET, M1, and $g_{d2}$ is the output conductance of the PMOSFET, M2. Gain degradation of differential amplifiers has been shown to be dominated primarily by $g_d$ degradation [5,7]. Therefore, in this paper, we will neglect the effect of $g_m$ degradation. Analog circuit reliability can thus be evaluated based on $\Delta V_{\text{offset}}$ and $\Delta g_d$.

Figures 4 and 5 show that both of these parameters are strong functions of measurement $V_{gs}$ and $V_{ds}$. Since analog circuits are designed with biasing conditions, $L_{\text{eff}}$, and circuit topography (cascade Vs non-cascade) as variables, hot-carrier reliability of analog circuits has to be based on a set of design curves that span the analog design space.

IV. HOT-CARRIER ANALOG DESIGN CURVES

During circuit operation, the gate voltage transients of analog circuits are small perturbations about the biasing condition (typically about a 100mV - 500mV swing). Unlike digital circuits, a duty cycle approach does not apply to analog circuits. Thus lifetime based on DC stress with analog biasing conditions would be approximately equal to analog circuit lifetime. High speed analog circuits require smaller $L_{\text{eff}}$ and larger biasing current for the differential pair in circuits such as figure 6. In this study, we have DC stressed single NMOSFETs with different $L_{\text{eff}}$ and with a gate voltage representative of analog biasing conditions ($V_{gs} - V_{T} = 0.1v - 0.5v$).

Offset Voltage

Figures 7 and 8 show the hot-carrier induced change in offset voltage of the circuit in figure 6 as a function of $L_{\text{eff}}$, with biasing current and biasing $V_{ds}$ as variables. For a fixed biasing $V_{ds}$ and biasing current, decreasing $L_{\text{eff}}$ from 5μm to 1μm increases hot-carrier induced $\Delta V_{\text{offset}}$ by approximately one order of magnitude. On the other hand, for a fixed $V_{ds}$ and a fixed $L_{\text{eff}}$, $\Delta V_{\text{offset}}$ increases by a factor of five as the biasing current is changed from 1μA/μm to 10μA/μm. If a specific analog application requires a maximum $\Delta V_{\text{offset}}$ of 10μV, then for a biasing current of 3μA/μm, $L_{\text{eff}}$ has to be greater than 2.5μm and for a biasing current of 5μA/μm, $L_{\text{eff}}$ has to be greater than 3.5μm.

Figure 7. Hot-carrier induced change in offset voltage, $\Delta V_{\text{offset}}$, as a function of $L_{\text{eff}}$ for different biasing currents. $\Delta V_{\text{offset}}$ is monitored at a measurement $V_{ds}$ of 1v. The solid lines are the projected $\Delta V_{\text{offset}}$ based on (4).

Figure 8. Change in offset voltage, $\Delta V_{\text{offset}}$, as a function of $L_{\text{eff}}$ for different measurement $V_{ds}$. $\Delta V_{\text{offset}}$ is monitored at a biasing current of 3μA/μm. Solid lines are projected values based on (4).

Figure 8 shows that for a fixed $L_{\text{eff}}$ and for a fixed biasing current, $\Delta V_{\text{offset}}$ decreases by almost an order of magnitude as we increase the biasing $V_{ds}$ from 0.7v to 2v. Figure 9 shows $\Delta V_{\text{offset}}$ as a function of stressing $V_{ds}$ (different from biasing $V_{ds}$) for different channel lengths. Stressing $V_{ds}$ represents the maximum voltage across M1 or M3 and is determined by supply voltage and circuit topography. The stressing voltage can be reduced by using cascode structures. Approximately two orders of magnitude improvement can be achieved by decreasing the stressing $V_{ds}$ from 5v to 4v.

$\Delta V_{\text{offset}}$ prediction model

Hot-carrier induced change in offset voltage of an NMOSFET differential pair can be expressed as [13]

$$\Delta V_{\text{offset}} = \Delta V_{T} - (\Delta \mu/\mu)(V_{gs} - V_{T})/2$$

(3)
where $\mu$ is the mobility of NMOSFET and $\Delta \mu$ (0 for NMOSFET) and $\Delta V_T$ (0 for NMOSFET) are the hot-carrier induced change in mobility and threshold voltage respectively. The fractional change in mobility and $\Delta V_T$ are proportional to $f(\text{Age})$, where Age, which represents the severity of hot-carrier damage, is a function of drain and substrate currents [3]. For a given amount of hot-carrier damage and at a fixed $V_{ds}$, $\Delta \mu/\mu$ is constant and the change in offset voltage increases with $V_{gs}$. Since bias current of the differential pair increases with $V_{gs}$, the offset voltage increases with $I_d/W$ in figure 7. For a fixed stressing $V_{ds}$, Age decreases with decreasing $L_{eff}$. Thus if we know the $\Delta V_{\text{offset}}$ of the minimum $L_{eff}$ case, then under identical biasing conditions, $\Delta V_{\text{offset}}$ of any $L_{eff}$ can be approximately calculated using the following relation

$$\Delta V_{\text{offset}}(L_{eff}) = \Delta V_{\text{offset}}(\text{min. } L) \cdot \frac{\text{Age}(L_{eff})}{\text{Age}(\text{min. } L)} \tag{4}$$

The solid lines in figures 7 and 8, which represent the projected $\Delta V_{\text{offset}}$ based on (4), show excellent correlation with experimental data. This can greatly simplify analog hot-carrier lifetime prediction. For a fixed amount of damage, as we increase measurement $V_{ds}$, some of the interface states become neutral and as a result both the terms in (3) decreases with increasing $V_{ds}$. This explains why $\Delta V_{\text{offset}}$ decreases with increasing $V_{ds}$ in figure 8.

Output conductance

Figure 9 shows the hot-carrier induced change in output conductance as a function of $L_{eff}$ for different biasing $V_{ds}$. An order of magnitude improvement in $g_d$ degradation can be achieved by changing biasing $V_{ds}$ from 0.7v to 1.5v. If we neglect the change in $g_m$ and assume that only M1 in figure 6 suffers significant degradation, then from (2) fractional change in the gain of the differential amplifier of figure 6 can be expressed as

$$\frac{\Delta G}{G} = -\frac{\Delta g_m}{g_m} \left( \frac{8d1}{(8d1 + 8d2)} \right) \tag{5}$$

In most cases, analog circuits are robust enough to withstand a large gain degradation but has to meet a very tight offset voltage requirement. Thus hot-carrier reliability of analog circuits will be limited primarily by $\Delta V_{\text{offset}}$.

V. DIGITAL VS ANALOG LIFETIME

Figure 10 compares the digital and analog circuit lifetime in a mixed analog/digital technology. A fair comparison of digital and analog circuit parameters can only be made if appropriate stressing conditions are used. Digital circuit lifetime is determined by stressing NMOSFETs under maximum interface state generation condition (peak Age) and then using appropriate time factor (NTF) as shown in section II. Digital circuit speed degradation can be obtained by dividing the saturation or linear drain current change by the appropriate speed factor, typically 4 if $I_{dsat}$ is used as the monitor and typically 8 if $I_{lin}$ is used as monitor. Analog circuit lifetime is determined by stressing devices with $(V_{gs} - V_T) = 0.1v - 0.3v$.

From figure 10 we see that in 10 years, $I_{dsat}$ of an NMOSFET within a digital circuit changes by about 9% for 50MHz operation. On the other hand, if an $L_{eff}$ of 1$$m$ is used for differential pairs in analog circuits, $\Delta V_{\text{offset}}$ changes by about 40mV in 10years. A factor of 5 improvement can be obtained by changing $L_{eff}$ from 1$$m$ to 3$$m$. It then becomes extremely important for reliability engineers and analog circuit designers.
to evaluate performance and hot-carrier reliability tradeoffs using the design curves presented in this paper. Since analog circuits are extremely sensitive to matching characteristics, reliability simulators such as BERT (BERkeley Reliability Tools) [14] becomes indispensable for accurate reliability prediction of analog circuits.

VI. NMOSFET VS PMOSFET DIFFERENTIAL PAIRS

Figure 11 compares the hot-carrier induced $\Delta V_{\text{offset}}$ of a PMOSFET differential pair with that of an NMOSFET differential pair. The stressing and measurement conditions are identical in both cases. The PMOSFET offset voltage shows an much larger degradation than the NMOSFET case. This can be explained by the substrate and gate current characteristics shown in figure 12. The analog bias window for PMOSFET overlaps the peak $I_g$ region while the NMOSFET bias window is away from the peak NMOSFET degradation region. Thus the PMOSFET differential pair will be subjected to a more pronounced hot-carrier aging, and therefore, a larger $\Delta V_{\text{offset}}$.

VII. ANALOG DEGRADATION MECHANISM

Although analog circuit biasing condition (low $V_{gs}$) favors hole injection, in our study, the analog device parameter degradation was dominated by interface states for measurement $V_{ds} < 2v$. For $V_{ds} > 2v$, most of the interface states become neutral and we noticed some hole trapping effect. The impact of hole trapping on analog circuit degradation can be a function of technology and requires further study.

VIII. CONCLUSION

Hot-carrier reliability of analog circuits is found to be a very sensitive function of biasing current, channel length and biasing $V_{ds}$. High speed analog applications which require smaller channel length can minimize the hot-carrier sensitivity by reducing the biasing current and by increasing the biasing $V_{ds}$. Almost two orders of magnitude improvement in $\Delta V_{\text{offset}}$ degradation can be achieved by reducing the stressing $V_{ds}$ by 1v. While digital circuit parameter $I_{sat}$ changed by 9% in 10 years, an $L_{eff} > 3.5 \mu m$ is needed to achieve a $\Delta V_{\text{offset}}$ of less than 10mV on the same technology in 10 years. Reliability simulators, such as BERT, can be extremely useful for accurately predicting analog circuit reliability.

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