Characterization of Hot-Carrier Effects in Thin-Film Fully-Depleted SOI MOSFETs

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ABSTRACT

Previous conflicting reports concerning fully-depleted SOI device hot electron reliability is partially due to misunderstanding over the maximum channel electric field (E_m). Experimental results using SOI MOSFETs with body contacts indicate that E_m1 is just a weak function of thin-film SOI thickness (T Si) and E_m can be significantly lower than in a bulk device with drain junction depth (X D) comparable to T Si. The theoretical correlation between SOI MOSFET's gate current and substrate current are experimentally verified. This provides a means (I C) of studying E_m in SOI device without body contacts. Both N- and P-MOSFETs can have better hot-carrier reliability than comparable bulk devices. Thin film SOI MOSFETs have better prospects for meeting breakdown voltage and hot-electron reliability requirements than previously thought.

I. INTRODUCTION

Thin-film fully-depleted (FD) SOI MOSFETs have attracted much attention because of their large drain saturation current, absence of kink effect, and superior subthreshold leakage. However, as far as device reliability and breakdown voltage are concerned, previous reports are divided on whether FD SOI devices have reduced or enhanced hot-carrier susceptibility and sensitivity to SOI film thickness [1]-[7]. The main difficulty is that substrate current, (I SUB), the convenient monitor of channel field for bulk MOS devices, cannot be measured on the SOI devices with floating body. While gate current has been suggested as a lifetime parameter for SOI N-MOS devices [6], gate current is difficult to measure and gate current has not been confirmed as a valid monitor of channel field without substrate current [7]. In this study, for the first time, using a special SOI device structure with body contact, both substrate (body) current (I SUB) and gate current (I G) were directly measured in the same devices. Based on this experiment, not only is the channel field in SOI devices quantified, but also the correlation between I SUB and I G is established. Finally, the hot carrier degradation lifetimes of SOI N- and P-MOSFETs are compared with those of bulk devices.

II. EXPERIMENTS

FD N- and P-channel SOI devices were fabricated on SIMOX wafers using a CMOS process. The buried oxide thickness is about 3500 Å, LOCOS isolation and 3000 Å in-situ doped N+ poly gate were used. To collect I SUB, the N-MOS devices have a special P+ region to contact the P-type body, as illustrated in Fig.1. The P+ region was formed by P-MOS S/D implant (B11, 4x10^15 cm^-2, 30 keV). Similarly, P-MOS devices have an N+ region to contact N-type body using N-MOS S/D implant (As, 4x10^15 cm^-2, 70 keV). The measured I SUB in these structures is found to be proportional to the channel width, indicating a high efficiency in collecting I SUB.

Fig.1 A schematic of the body contact in N-MOS SOI devices. SOI P-MOS devices have the similar structure with N+ and P+ regions exchanged.

III. RESULTS AND DISCUSSIONS

(A) Analytical Hot-Carrier Models

In bulk MOSFETs, the maximum channel field can be estimated as follows [8]:

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\[ E_m = \frac{(V_D - V_{DSAT})}{\ell} \]  \hspace{1cm} (1)

\[ \ell = 0.22 \cdot T_{OX}^{1/3} \cdot X_j^{1/2} \]  \hspace{1cm} (2)

where \( X_j \) is the drain junction depth and \( \ell \) is the characteristic length. The hot-carrier currents, \( I_{SUB} \) and \( I_G \), can be expressed as follows [9]:

\[ I_{SUB} = \frac{A_i}{B_i} (V_D - V_{DSAT}) I_D \exp\left(-\frac{B_i}{E_m}\right) \]  \hspace{1cm} (3)

where \( A_i \) and \( B_i \) are known constants for impact ionization rate of channel carriers [9]. \( B_i \) is around \( 1.7 \times 10^6 \, \text{V} \cdot \text{cm}^{-1} \) for electrons and \( 3.7 \times 10^6 \, \text{V} \cdot \text{cm}^{-1} \) for holes [10].

\[ I_G = C_1 (E_{ox}) I_D \exp\left(-\frac{\varphi_b}{E_m \lambda_e}\right) \]  \hspace{1cm} for N-MOS, \hspace{1cm} (4)

\[ I_G = C_2 (E_{ox}) I_{SUB} \exp\left(-\frac{\varphi_b}{E_m \lambda_e}\right) \]  \hspace{1cm} for P-MOS, \hspace{1cm} (5)

where \( \varphi_b \) is the barrier height at Si/SiO\(_2\) interface for electron, \( \lambda_e \) is the scattering mean-free path of electron. It is worth noting that the gate current of P-MOSFET's results from electron injection rather than hole injection into the oxide in the low-\( V_G \) regime [11].

From Eqs. 3, 4, and 5, we find:

\[ \ln\left(\frac{I_{SUB}}{I_D (V_D - V_{DSAT})}\right) = \ln\left(\frac{A_i}{B_i}\right) - \frac{B_i \ell}{V_D - V_{DSAT}} \]  \hspace{1cm} (6)

\[ \frac{I_G}{I_D} = \frac{C (E_{ox}) B_i}{A_i (V_D - V_{DSAT})} \left(\frac{I_{SUB}}{I_D}\right) \frac{\varphi_b}{B_i \lambda_e} \]  \hspace{1cm} for N-MOS \hspace{1cm} (7)

\[ \frac{I_G}{I_{SUB}} = \frac{C (E_{ox}) B_i}{A_i (V_D - V_{DSAT})} \left(\frac{I_{SUB}}{I_D}\right) \frac{\varphi_b}{B_i \lambda_e} \]  \hspace{1cm} for P-MOS. \hspace{1cm} (8)

(B) Hot-Carrier Currents and Channel Electric Field

In SOI devices, whether Eq. 1 and Eq. 2 can be used and how are not clear. Colinge [3] used \( T_{si} \) as a substitute for \( X_j \) in Eq. 2 to estimate the channel field, while Chen, et al. [6] reported that this overestimates \( E_m \). From Eq. 6, a plot of \( \ln(I_{SUB}/(I_D (V_D - V_{DSAT})) \) versus \( 1/(V_D - V_{DSAT}) \) should yield one straight line for all bias voltages, for both N- and P-MOSFETs, as shown in Fig.2. The slope of this straight line gives \( B_i \ell \), from which \( \ell \) and hence \( E_m \) can be determined experimentally. It is found that using thin film SOI thickness \( T_{si} \) as a substitute for \( X_j \) can overestimate \( E_m \) by a factor of 2 for both N- and P-MOS devices (roughly equivalent to overestimating \( V_D \) by more than 50%).

\[ \text{Fig.2 Experimental determination of the characteristic length } \ell \text{ in } E_m = \frac{(V_D - V_{DSAT})}{\ell} \text{ in SOI and bulk devices. (a), N-MOS devices: For bulk device, the measured } \ell \text{ is 461 Å. For SOI device, the measured } \ell \text{ is 1194 and 1254 Å, while the } \ell \text{'s, based on the bulk MOSFET } E_m \text{ model with } X_j = T_{si} \text{ are 554 Å and 616 Å. (b), P-MOS devices: For bulk device, the measured } \ell \text{ is 426 Å. For SOI device, the measured } \ell \text{'s are 1213 and 1271 Å, while the } \ell \text{'s, based on the bulk MOSFET } E_m \text{ model with } X_j = T_{si} \text{ are 554 Å and 616 Å. The data clearly show that } E_m \text{ in SOI devices can be much lower than in bulk devices.}

It can be deduced from Eq.3 that \( I_{SUB}/I_D \) is a simple monitor of the maximum channel field \( E_m \). Fig.3(a) and (b) show the distribution of measured \( I_{SUB}/I_D \) for the N-MOS SOI.
and bulk devices, respectively. Although $T_{Si}$ variation across a wafer is as high as 200 Å, the $I_{SUB}/I_D$ variation is only ±10% and comparable to the ±10% variation in the bulk case, confirming the weak $E_m$ dependence on $T_{Si}$. Besides, SOI devices have much lower $I_{SUB}/I_D$, hence $E_m$, by a factor of 4 than comparable bulk devices (see Fig1(a) and (b)), although $V_{DSAT}$ are about the same. $T_{Si}$ was determined by the CV technique [12].

![Graph](image1)

(a)

![Graph](image2)

(b)

**Fig.3** Distribution of $I_{SUB}/I_D$ of (a) SOI, and (b) bulk N-MOS devices. Both $I_{SUB}$ and $I_D$ were measured at the maximum $I_{SUB}$ point with $V_D=4$ V. The $I_{SUB}/I_D$ sensitivity to SOI $T_{Si}$ is very weak. The variations of $I_{SUB}/I_D$ across both wafers are about ±10%. SOI devices have lower $I_{SUB}/I_D$ hence $E_m$ by a factor of 4 than the comparable bulk MOSFETs.

The P-MOS data is shown in Fig.4. It can be seen that the measured $I_{SUB}/I_D$ is also a weak function of $T_{Si}$. The $I_{SUB}/I_D$ values for the SOI P-MOS devices are lower than that in the bulk devices even though the SOI devices have a thinner gate oxide. Since the gate current in P-MOS devices is much larger as compared to that in N-MOS devices thus easier to be measured, the $I_{G}/I_D$ data is also presented in the same figure. Clearly, the electron injection into the gate oxide is also a weak function of the $T_{Si}$. Besides, the $I_{G}/I_D$ values for the SOI devices are a little higher than the bulk devices probably because the vertical field of gate oxide on the SOI devices is higher than on the bulk devices.

![Graph](image3)

(a)

![Graph](image4)

(b)

**Fig.4** Distribution of $I_{SUB}/I_D$ and $I_{G}/I_D$ of (a) SOI, and (b) bulk P-MOS devices. $I_{SUB}$, $I_G$ and $I_D$ were measured at the maximum $I_{SUB}$ point with $V_D=-5$ V. The $I_{SUB}/I_D$ and $I_{G}/I_D$ sensitivity to SOI $T_{Si}$ is very weak. SOI devices have lower $I_{SUB}/I_D$ and hence $E_m$ than the bulk MOSFETs.

Fig.5 demonstrates the combined effects of 2D and lateral doping gradient in drain region. The channel field increase exponentially due to the 2D effect, while decreases near the drain region due to the lateral doping effect. Both the lower $E_m$ and weaker dependence on $T_{Si}$ in thin film SOI devices can be attributed to the lateral drain doping gradient [13]. Simulations found relatively low $E_m$ and weak $E_m$ sensitivity on $T_{Si}$ within the range of interest (500–1100 Å). $E_m$ is a function of the lateral drain doping gradient even for non-LDD As drains. In
the case of bulk MOSFETs, the doping gradient varies with \( X_j \); this contributes to the \( E_m \) dependence on \( X_j \). In the case of SOI MOSFETs, lateral doping gradient is decoupled from \( X_j \) (or \( T_{si} \)). Therefore, \( E_m \) can be lower in an SOI device than a bulk device with small \( X_j = T_{si} \) and a weak dependence on \( T_{si} \) as well.

![Graph](image1.png)

**Fig.5** Demonstration of the 2D and lateral drain doping gradient effects on channel electric distributions in a MOS device. The lateral doping gradient \( L \) is defined as

\[
L = \left( \frac{1}{N_D} \frac{dN_D}{dy} \right)^{-1}
\]

at around \( N_D = 1 \times 10^{18} \text{ cm}^{-2} \).

(C) **Hot-Carrier Effects**

\( I_{SUB} \) and \( I_G \) are correlated to each other by a power-law relationship, because both of them are exponential functions of \( E_m \) in equations 3, 4 and 7 [14],[15]. Fig.6 demonstrates the relationship between \( I_{SUB} \) and \( I_G \) in SOI N-MOS devices. Based on equation 7, to the first order, the \( \log(I_G/I_D) \) versus \( \log(I_{SUB}/I_D) \) plot is a function of only oxide field, \( E_{ox} = (V_G - V_D)/T_{ox} \), and its slope is equal to \( \varphi_b / (B_1 \lambda) \). This slope is 2.1 suggesting that \( B_1 \lambda \), i.e., the critical electron energy for impact ionization, is about 1.5 eV if we assume the Si/SiO2 barrier height for electrons is \( \varphi_b = 3.1 \text{ eV} \). This result agrees very well with the bulk case [15]. The agreement between theoretical prediction and experimental data suggests that \( I_G \) can be used as a monitor of \( E_m \) for SOI N-MOS devices with the body contacts, e.g., \( \ell \) can be estimated from the slope of the \( \log(I_G/I_D) \) versus \( 1/(V_D^2 V_{DSAT}) \) plot.

![Graph](image2.png)

**Fig.6** Correlation between \( I_{SUB} \) and \( I_G \) in SOI N-MOS devices. The slope is about 2.1. Based on the expression (4), the slope approximately equals to \( \varphi_b / (B_1 \lambda) \) from which \( B_1 \lambda \) can be calculated.

Previous reports are divided on whether FD SOI devices are less [3]-[7] or more [1], [2] vulnerable to hot-carrier effects. The fact that FD SOI devices often have a lower channel field \( E_m \) than bulk devices due to a more graded drain doping profile should also be reflected from the device degradation in terms of hot-carrier stress. In addition, Fig.7 shows the saturation drain current shifts for a given maximum \( I_{SUB} \) is not larger in SOI than bulk N-MOS devices. Fig.8 shows the extrapolated lifetime for both SOI N- and P-MOS devices, respectively, as compared to the bulk devices. The devices were stressed under the worst-case stress conditions (maximum \( I_{SUB} \) for N-MOS case and maximum \( I_G \) for P-MOS case). Although \( X_j \) for the bulk devices is as large as 2000 Å, the SOI devices with \( T_{si} = 800 \) Å are still slightly less vulnerable than the bulk devices to hot-carrier degradation at least in this case study.

![Graph](image3.png)

**Fig.7** Comparison of the saturation drain current shifts for a specific maximum \( I_{SUB} \) stress between the SOI and bulk N-MOS devices.
ACKNOWLEDGMENT

This work was supported by SRC, TI, Rockwell International under California state MICRO program, and AFOSR/CEMIP under contract F49620-90-0029.

REFERENCES


IV. CONCLUSIONS

In conclusion, channel field in SOI MOSFETs is lower than previously assumed. Hot-carrier degradation of thin film FD SOI devices can be less severe than a similar bulk MOSFET. The decoupling of SOI MOSFET junction depth (T_J) and lateral doping gradient is little discussed but of significant advantage in design engineering. This realization improves the prospects of thin film SOI devices meeting breakdown voltage and hot-carrier effects requirements. The correlation between I_{SUB} and I_G is confirmed and suggests that the channel field may be characterized through the measurable I_G. I_G measurement should help drain structure design engineering.