SOI MATERIAL TECHNOLOGY USING PLASMA IMMERSION ION IMPLANTATION


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Silicon on insulator (SOI) devices has many attractive applications in integrated circuit technology. The high cost of manufacturing the SOI wafers, however, prevents it from being widely accepted for massive production. Separation by plasma implantation of oxygen (SPIMOX), an extremely high throughput SIMOX formation process using plasma immersion ion implantation (PIII) has demonstrated promising results. In this paper, improvement on SPIMOX process is presented. High-dose implantation is a costly procedure for “smart cut” process. A low cost, high throughput implantation by hydrogen or helium plasma is demonstrated as a feasible, novel process for SOI technology using PIII.

SPIMOX wafers are fabricated using an oxygen plasma from an ECR plasma source operating at 2.45 GHz. There are a few physical limitations in the plasma implantation process as shown in the phase diagram in Figure 1, namely: i) oxygen gas breakdown at high voltage; ii) collisionless sheath to preserve single energy implantation; iii) ion density limit from oxygen density; and iv) heat dissipation capability. Currently, the oxygen plasma is generated at 0.05 to 0.1 mTorr oxygen pressure and 350 W microwave power. The implantation is carried out at 60 ~ 70 kV for 3 ~ 6 minutes to achieve a nominal dose of 1 ~ 2 x 10^{17} cm^{-2}.

The secondary ion mass spectroscopy (SIMS) spectra of the as-implanted and high temperature annealed SPIMOX samples are shown in Figure 2. The implanted species is dominated by O_2+ instead of O+ in the plasma used for implantation as indicated by the oxygen peak at 60 nm underneath the Si surface. After annealed at 1325 °C for 3 hours, a complete buried oxide (BOX) layer is formed. The stoichiometry of the BOX layer is identical to the passivation layer deposited at the wafer surface. The annealed sample SIMS spectrum shows sharp Si/oxide interface. A cross-sectional transmission electron microscopy (XTEM) micrograph of the annealed SPIMOX sample is shown in Figure 3. As seen, continuous buried oxide layer is formed under a single crystal Si over-layer.

The process conditions have to be optimized to find the best operation condition for SPIMOX process. Figure 4 shows a couple of XTEM micrographs from non-ideal process conditions. Extra high dose (2.5 x 10^{17} cm^{-2}) implantation causes high oxygen concentration in the top Si, and oxide inclusions is formed in the annealed sample as shown in Figure 4 (a). In Figure 4 (b), when the annealing temperature is not high enough (1250 °C only), wavy Si/oxide interface is formed.

For the “smart cut” process, Figure 5 shows the microcavity formation in Si from the PIII helium implantation at 34 kV and subsequent 30 minutes, 1050 °C annealing. SOI structure shown in Figure 6 is formed by the “smart cut” process using PIII implantation: 1 x 10^{17} cm^{-2} helium is implanted into Si substrate at 33 kV. The implanted wafer is then base-bathed and hydrophobically bonded with an oxide/nitride coated substrate at room temperature. The implanted wafer cracked along the implanted helium peak region at subsequent 500 °C annealing. The SOI structure is finally annealed at 1100 °C for 60 minutes to solidify the bonding. Similar results are achieved using hydrogen plasma implantation.

SOI wafers have been successfully fabricated by SPIMOX process using oxygen plasma. Si over-layer crystallinity is preserved and sharp Si/oxide interface is formed. Dramatically reduced production cost in SPIMOX can lead to low-cost and high-volume production of SOI wafers using this technique. Hydrogen and helium plasma implantation is demonstrated for “smart cut” process using PIII. This work is sponsored in part by the Joint Services Electronics Program, Contract Number F49620-94-C-0038 and National Science Foundation, Grant Number ECS-9202993.

References
Figure 1. SPIMOX process implantation phase space diagram.

Figure 2. SIMS profile of the oxygen concentration of as-implanted and annealed wafer formed by SPIMOX.

Figure 3. XTEM micrograph of the SOI structure formed using the SPIMOX process. The implantation was carried out at 60 kV. The wafer was annealed at 1325 °C for 3 hours.

Figure 4. Non-ideal SPIMOX processes: (a) oxide inclusions in Si over-layer due to extra high dose implantation; (b) wavy Si/oxide interface caused by not high enough annealing temperature (1250 °C).

Figure 5. Microcavity formation in Si from PIII He implantation (34 kV, 2x10^17 cm^-2) and subsequent 30 min. 1050°C annealing.

Figure 6. SOI structures formed by the Smartcut process using PIII He implantation.