Investigation of Interconnect Capacitance Characterization using Charge-Based Capacitance Measurement (CBCM) Technique and 3-D Simulation

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Abstract
This paper examines the recently introduced Charge-Based Capacitance Measurement (CBCM) technique through use of a 3-D interconnect simulator. This method is shown to have several advantages over extensive computer simulation in determining parasitic interconnect capacitances, which are the dominant source of delay in modern circuits. Metal to substrate, interwire, and interlayer capacitances are each discussed and overall close agreement is found between CBCM and 3-D simulation. Full process interconnect characterization is one possible application of this new compact, high-resolution test structure.

Introduction
In the past, circuit delay has been due mostly to transistors. For this reason, much effort is put into device scaling. Today, the dominant source of delay in circuits such as ASIC's and microprocessors is metal interconnect. As interconnect scales with each technology generation, several tradeoffs are made. In order to reduce line resistance and improve electromigration properties, metal height is kept fairly constant, and not scaled with pitch. The increasing aspect ratio (height/pitch) results in larger coupling capacitances and more crosstalk. This problem worsens as more metal layers are added with almost every generation. The performance gains of adding more metalization layers will soon saturate; in other words, a limit exists for the number of metal layers feasible for integrated circuits. Once this limit is reached, only tighter pitches in each layer will result in higher density, leading to larger capacitances again [1].

From these points, it can be seen that interconnect capacitance characterization is an important aspect of current and future process development as well as circuit design. In order to give circuit designers an accurate assessment of speed and noise issues, parasitic capacitances due to interconnect must be well described. Currently, this is done with extensive computer simulation. A new, measurement-based technique, Charge-Based Capacitance Measurement (CBCM) [2], has been developed to characterize interconnect capacitances. This simple, compact, and sensitive test structure can be used to measure any interconnect capacitance structure. In this paper, we will compare the results from CBCM to those obtained by RAPHAEL, a capacitance simulation package [3].

Metal to Substrate Capacitances
A test chip was fabricated in an industrial 0.8 μm, double metal technology with many interconnect test structures. An example of the test structure used is shown in figure 1. V1 and V2 are non-overlapping waveforms, eliminating short-circuit current. The difference between the measured currents I and I' will be proportional to the capacitance being measured. With properly designed test structures, the resolution limit of CBCM is determined by the matching of the two pseudo-inverters. This limit has been estimated in [2] to be 0.01 fF.

The first, and simplest, structure to characterize is that of an isolated metal line over substrate. By varying the width of the line with a constant length, a linear capacitance versus linewidth plot results, from which area and fringing components of the capacitance can be found. Figure 2 shows metal 2 capacitance to substrate as a function of drawn width for both measurement and simulation. It can be seen that the intercepts of the two lines are essentially identical, while the slopes are different. The slope in this figure corresponds to the area component of the capaci-

![Figure 1](image_url)

Figure 1. Test structure used to measure parasitic interconnect capacitances. In this case, a metal 1 to metal 2 overlap capacitance is being measured.

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Fig. 2. Metal 2 capacitance over silicon substrate as a function of drawn width. Area and fringing components of the total capacitance are extracted and given in the inset table.

Fig. 3. Extraction methodology for $C_{\text{interwire}}$ on this test chip.

Discrepancies between RAPHAEL and CBCM may result in this case from substrate effects that are not taken into account in the simulator. RAPHAEL incorporates a metal ground plane, rather than a doped substrate, in its calculations. Metal-oxide-silicon capacitance has different characteristics than metal-oxide-metal does. Small changes in capacitance could result due to inversion in the field regions, or other substrate effects. This is an inherent advantage of measurement in the case of metal to substrate capacitance. Also, the interconnect structures used in the test chip were fairly long ($L = 135 \mu m$) compared to their width. A long, thin metal line will have a much larger fringing component of capacitance than area component. This fact makes the measurements particularly sensitive to $C_{\text{area}}$. In the future, structures of this type should be designed with roughly similar areas and perimeters to avoid potential errors.

**Interwire Capacitances**

Capacitance between metal lines of the same layer is referred to as interwire, or coupling capacitance. As mentioned earlier, this is a major problem in current and future technologies due to tighter pitch and higher metal aspect ratios. This coupling between lines is commonly referred to as cross-talk. The presence of another nearby line will increase the total capacitance of an isolated line, which was discussed in the previous section. This added capacitance must be taken into account when routing global signals such as clocks, determining driver sizes and line widths/spacings, etc. In this test chip, our interwire structures were designed to measure this additional capacitance brought on by the presence of a neighboring wire. Figure 3 shows our methodology in extracting interwire capacitance. Figure 4 presents measurement and simulation data for 4 different spacings of metal 2 wires. The maximum added capacitance is around 2 ff per 135 $\mu m$ length. The general trend for both CBCM and RAPHAEL is an approximate $1/d^2$ relationship, where $d$ is the distance between lines. Using a small set of CBCM structures, a simple analytical fit could be made for $C_{\text{interwire}}$. Implementing this expression in a layout extraction program, very accurate capacitance values for long parallel lines could be calculated.

The minimum spacing of second level metal used in our test chip was 2 $\mu m$. In current technologies, minimum spacing between second level metal is normally 0.5 $\mu m$. Thus, the added capacitance of about 2 ff/135 $\mu m$ in our case will be significantly larger. For higher metal layers, interwire effects are more pronounced due to increased metal heights, and lessered substrate effects. Since most signals are routed on lower levels, crosstalk does not become critical in higher layers normally carrying power and ground. An additional layout method of reducing crosstalk is to include upper and/or lower ground planes surrounding the signals of interest. In the case of parallel metal 1 lines, a grounded metal 2 plate above the 2 lines would divert field lines to the ground plane rather than the neighboring signal. A tradeoff is made here, as total capacitance on
Interlayer Capacitances

Interlayer capacitances are significant, especially in the case of wide lines or long, dense arrays. An assumption made in many analytical interconnect models to provide simplicity is that an array of lines behaves the same as a continuous plate when dealing with interlayer capacitances [6]. We tested this assumption by placing metal one lines increasingly closer together underneath a metal 2 plate. We then measured the capacitance on the metal 2 plate. Each overlap was 1.5 μm x 2 μm, and spacings between metal one lines were 1.5 μm, 3 μm, and 4.5 μm. We found a saturating effect where capacitance was only increased by a few percent when decreasing spacing from 3 to 1.5 μm. Figure 5 shows our data compared to RAPHAEL simulations. Simulations show a similar saturating effect, although it takes place more gradually, or equivalently, at smaller spacings.

Interlayer capacitances, more than previous structures, bring into focus one major flaw in interconnect simulations; it is difficult to generate exact input files due to the variance of inter-level dielectric (ILD) thicknesses. Without taking SEM measurements of each structure, it is impossible to simulate interlayer capacitances with complete accuracy. In this case for example, as metal 1 lines become more dense, ILD thickness between first and second level metals is known to become thicker as a result of processing conditions. While the ILD is thickest when spacing is minimum (1.5 μm), it will be somewhat thinner in the case of 3 and 4.5 μm spacing. In this analysis, an ILD thickness corresponding to dense metal 1 was used. This results in the slight under-shoot by RAPHAEL at 18 and 24 lines. By varying the ILD thickness within given process specifications, a range of capacitances can be determined, and can be seen from the error bars in figure 4 to result in better agreement with CBCM. CBCM implicitly takes any ILD variation into account since it is based on measurement data. As a result of using CBCM, we estimate that a metal density of 33% or greater (spacing = 2 * width) can be approximated as a plate with negligible loss of accuracy.

Conclusions

This paper demonstrates the accuracy of the recently introduced CBCM method of characterizing interconnect structures. Important trends in interwire capacitance and saturation effects in interlayer geometries that were previously simulated using a 3-D simulator are verified by CBCM. Furthermore, several shortcomings of computer simulation in characterizing interconnect are pointed out. Other advantages of our new method include the extremely small size of the test structure, the ease of measurement setup, and a resolution limit around 0.01 fF. Potential
applications include full interconnect characterization of a given process, and scribe-line implementation to monitor fluctuations in that process. Work is underway to use CBCM in providing circuit designers with more accurate technology files for layout extraction, yielding more realistic simulation results.

References
4. MOSIS parametric test results, IHP-CMOS26G process.