High Current Effects in Silicide Films for Sub-0.25 μm VLSI Technologies

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Abstract - **Characterization and modeling of high current conduction in $TiSi_2$ and $CoSi_2$ films formed on n+ Si and n+ poly-Si under DC and pulsed stress conditions is reported for the first time. High current conductance of silicides is shown to be strongly affected by the technology and process conditions. The non-linear I-V characteristics of silicide films under DC and pulsed high current stress has been modeled and the non-linearity has been shown to be due to self-heating. Two physical parameters, B and λ, associated with DC and pulsed current stress, have been shown to be able to describe the sensitivity of the films to high current conduction. At high currents, an abrupt lowering of the resistance of the silicided structures is observed. Detailed analysis of the evolution of this resistance drop has been made. It is shown that the cause is related to the melting of the structures, which also causes degradation in the post-stress silicide film resistance. The critical current for these failures have been shown to be strongly influenced by the silicide film width and the time duration of the pulse. $CoSi_2$ films and films on poly-Si are shown to be more sensitive to high current conduction and degradation.**

1. Introduction

Continuous scaling of VLSI devices into the deep sub-micron region has led to the increased use of silicided metalization schemes for low-resistivity gates, interconnections and contacts between the metal and Si. Currently, self aligned silicide (salicide) processes are widely used in advanced CMOS technologies as shown in Fig. 1. In addition to lowering the gate sheet resistance (and therefore RC delay), they also reduce the source/drain parasitic resistance, by forming ohmic contacts in the source/drain regions of MOS transistors, thereby increasing the drive current of the transistors. Further, silicided diffusion structures are frequently used as resistors in I/O buffers and ESD protection circuits. These silicide films are often subjected to high current stress in MOS devices and as well as during electrostatic discharge (ESD) and electrical overstress (EOS) events. The thickness of the silicide is known to significantly impact ESD performance [1]. Failure of CVD W and force-fill Al contacts to silicided diffusions under high current stress has already been shown to initiate due to the degradation of the silicide under the contact plug [2]. Recently, the silicide thickness has also been shown to affect the contact resistance sensitivity to temperature and current [3]. The purpose of this work is to characterize and model high current effects in the two commonly used silicides

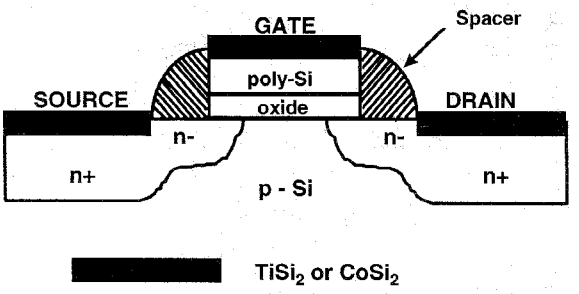


Fig. 1 Cross section of a salicided LDD NMOSFET.

namely, $TiSi_2$, and $CoSi_2$, under DC and pulsed conditions and evaluate the electrical and thermal stability of these structures. Currently, there is limited information available on the high current and self-heating effects [4,5] in these silicides. This paper will present a model and identify important parameters related to the high current behavior in silicides. An understanding of these high current effects will enable the impact of technology scaling of silicide films to be defined for the development of future deep sub-micron technologies.

2. Experimental

$TiSi_2$ and $CoSi_2$ films of different geometries and 50 nm thickness were formed using the salicide process for a state-of-the-art, 0.18 μm, 1.5 V, CMOS technology on n+ Si and n+ poly-Si. The various technology and process splits used in this work are summarized in Table 1. The sheet resistance values were measured with a four point probe test structure. The $TiSi_2$ films were formed after the gate-etch, followed by either a Ge pre-amorphization implant (PAI) or a Mo implant for improved sheet resistivity [6,7].

Silicide	Thickness	Si-Type	Implant Species	Sheet Resistance
$TiSi_2$	50 nm	n+ Si	Ge (PAI)	~ 3.0 Ω/□
		n+ polySi		~ 3.2 Ω/□
$TiSi_2$	50 nm	n+ Si	Mo	~ 3.2 Ω/□
$CoSi_2$	50 nm	n+ Si	N/A	~ 5.2 Ω/□
		n+ polySi	N/A	~ 5.5 Ω/□

L/W = 25/5, 50/5, and 10/2

Table 1 Silicide technologies, processes and sample geometry used in this work.

Fig. 2a shows the schematic cross sectional view of the silicide film on n+ Si. A lumped circuit representation of this

silicide structure is shown in Fig 2b. The temperature coefficient of resistance (TCR) were measured to be 0.0029 ± 0.0001 and 0.0031 ± 0.0001 $^0C^{-1}$ for $TiSi_2$ and $CoSi_2$ films (formed on n+ Si) respectively at low DC current. The films were then subjected to high DC and current pulse stress. A standard transmission line [8] pulsing scheme was used to generate square current pulses of varying widths and amplitudes. The instantaneous voltage developed across the films were measured using a digital oscilloscope.

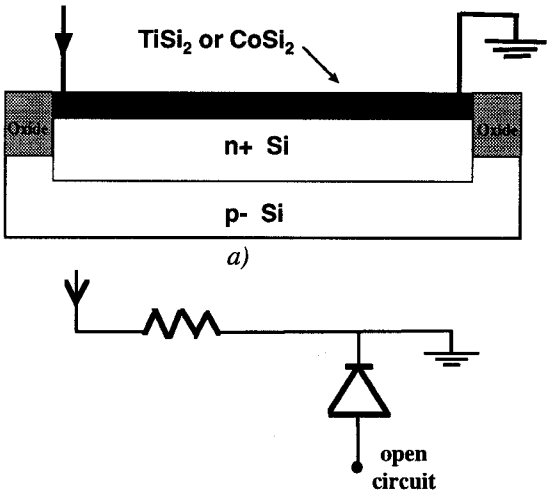


Fig. 2 a) Schematic cross section of silicide structures on n+ Si used in this study. b) A lumped equivalent circuit for the silicide structures.

3. Characterization and Modeling of High Current Effects in $TiSi_2$ Films

Characterization of High DC (steady state) Conduction

Fig. 3 shows the low DC current I-V characteristics for the $TiSi_2$ (Ge-PAI) on n+ Si structures with different L/W ratios. The curves indicate that under low current conditions the silicide films display ohmic behavior.

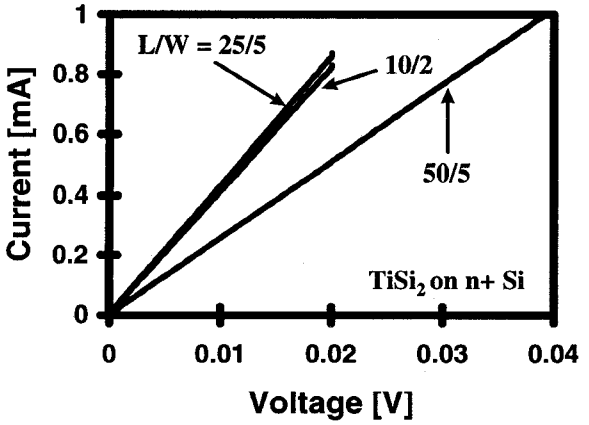


Fig. 3 Low current I-V characteristics for the $TiSi_2$ films on n+ Si showing ohmic behavior.

The high current I-V curves for these structures under DC stress conditions is shown in Fig. 4. The I-V curves become non-linear in the high current regime due to self-heating.

Model of Resistance Under DC High Current

Current conduction in thin silicide films under high DC stress conditions can be modeled as following. The voltage, V, across the film under high current, I, can be expressed as,

$$V = I \cdot R = I[R_0 + B(I \cdot V)] \quad (1)$$

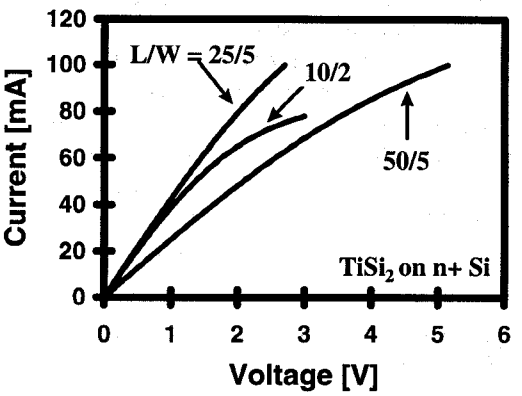


Fig. 4 High current I-V characteristics for the $TiSi_2$ films on n+ Si showing non-linear behavior.

where R_0 is the initial resistance of the film under low current stress. B is a parameter that depends on the sheet resistance, geometry, TCR, and thermal impedance of the structures and has the unit of Ω/Watt. Here, temperature rise is assumed to be proportional to the power dissipation, $I \cdot V$. Equation (1) can be rearranged to give,

$$R = \frac{R_0}{1 - BI^2} \quad (2)$$

The model developed as equation (2) has been used to fit resistance rise with current and is shown to be in excellent agreement with data as shown in Fig. 5.

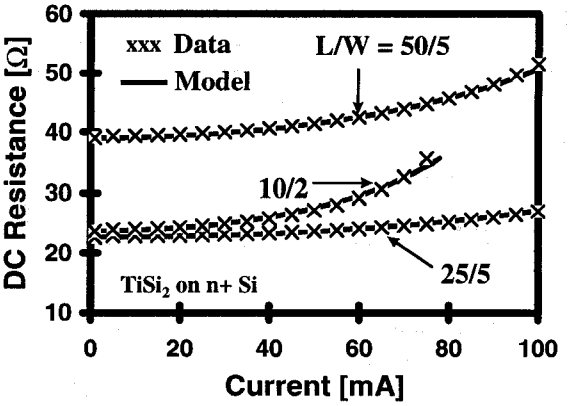


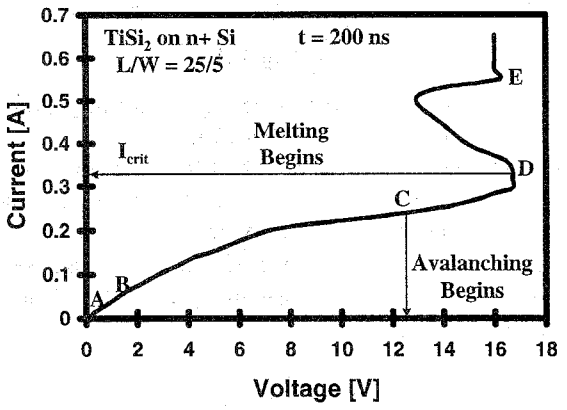
Fig. 5 The model for resistance as a function of current through the silicide is shown to be in excellent agreement with data for various geometry.

The values of B were found to be 16.5, 55, and 23 Ω/Watt for L/W = 25/5, 10/2 and the 50/5 respectively. Note that, B is

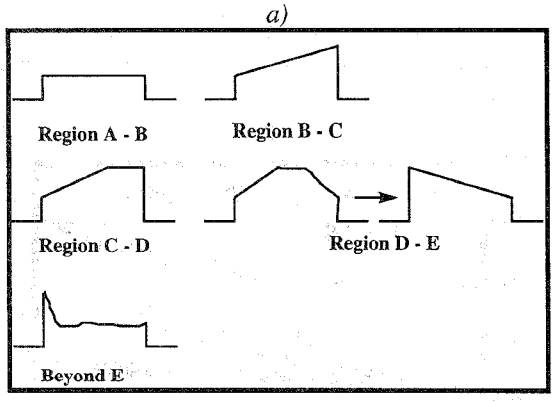
linearly dependent on the geometry (L/W) and thermal impedance of these structures. Although, the R_0 is identical for the 10/2 and 25/5 structures, thermal impedance and hence B for the 10/2 structure is higher due to the smaller surface area in contact with Si. In order to separate the design geometry effects from materials issues, B/R_0 for identical L/W, may be used while comparing different technologies and process effects.

Characterization of High Pulsed Current Conduction

Fig. 6a shows the high current I-V characteristics for a $TiSi_2$ film (L/W=25/5) on n+ Si measured with 200 ns pulses. The high current curve displays several characteristic regions as explained below. The instantaneous voltage pulse shapes in the various regions are shown in Fig 6b. The voltage was always measured at the end of the pulse. The post-stress resistance of the film was also monitored after each pulse with a small DC current. Fig. 7 shows the instantaneous resistance as a function of the pulse current corresponding to Fig. 6a with the different regions.



a)



b)

***Fig. 6** a) High current I-V characteristics for a $TiSi_2$ film under a 200 ns pulsed current stress. Voltage is measured at the end of the pulse. b) The voltage pulse shapes in the different regions of the I-V curve.*

In the region from A to B the curve is linear, as expected for a constant resistance. Beyond point B the I-V curve becomes non linear due to self heating of the silicide film and the voltage pulse can be observed to rise linearly with time [9]. At point C the underlying p-n junction begins to avalanche (at ~ 12.5 V determined experimentally in Fig. 20) and the voltage pulse saturates. As the magnitude of the current pulse is increased further, beyond point D, the voltage pulse begins to fall with time after rising sharply. At this point the junction begins to melt and as a result the silicide-Si interface begins to degrade causing an irreversible increase in the post-stress resistance of the film.

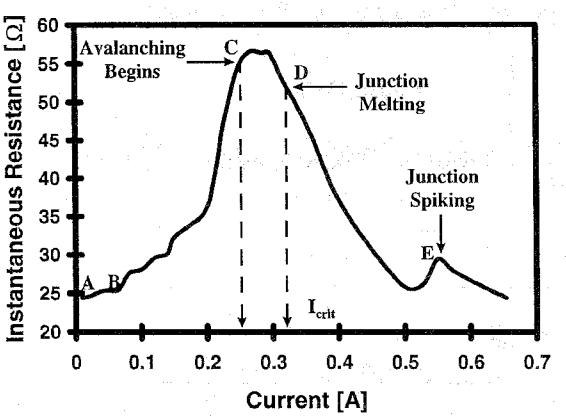


***Fig. 7** Instantaneous resistance of the silicide film as a function of the current amplitude for a 200 ns pulse stress.*

This threshold point of damage is defined as I_{crit}. At point E, the junction fails completely due to spiking and the voltage level remains at a constant high value until the structure fails like a fuse upon further increase in current. The effects beyond point C leading to failure are discussed in detail in section 5.

Model of Resistance Under Pulsed Current

The model for high current conduction under DC stress is now extended to include time dependence. This model can be used to describe the I-V characteristics up or close to point C, i.e., the onset of avalanching in the underlying p-n junction. Rewriting (1) as,

$$V = I \cdot R = I[R_0 + F \cdot \Delta T] \tag{3}$$

where F is a parameter that depends on the sheet resistance, geometry and TCR. The pulse energy can be expressed as,

$$E = \frac{1}{2} I^2 \cdot t \cdot (R_0 + R) = C_{th} \cdot \Delta T \tag{4}$$

where R_0 is the initial resistance at the beginning of the pulse (t = 0) and R is the resistance at the end of the pulse. C_{th} is the effective thermal capacity of the structure. Substituting ΔT from (4) in (3) gives,

$$R = R_0 \left(\frac{1+\lambda I^2}{1-\lambda I^2} \right) \tag{5}$$

where $\lambda = (Ft)/(2C_{th})$ in units of Ω/Watt or A^{-2}. The model developed in the form of (5) has been used to simulate high current conduction in the $TiSi_2$ film for two different pulse widths and the results are shown to be in good agreement with

data in Fig. 8. For the $TiSi_2$ film with L/W = 25/5, the values of λ were found to be 5.8 and 8.0 Ω/Watt for 200 ns and 500 ns pulse duration respectively. Increase in λ with t is not linear since the effective thermal capacity also increases with t, due to increasing heat diffusion into the surrounding.

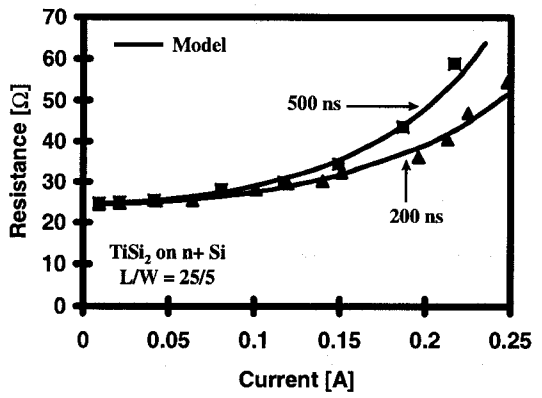


Fig. 8 High current conduction model for $TiSi_2$ films under pulsed stress conditions.

4. Technology and Process Dependence of High Current Conduction

In this section, effects of technology and processes on the high current conduction under DC and pulsed current stress conditions will be examined. First a $CoSi_2$ technology will be compared with the $TiSi_2$ technology discussed in the last section. Secondly, results of using Mo implant on the high current effects in $TiSi_2$ will be compared with that for the Ge-PAI $TiSi_2$ process discussed in the last section. Finally, high current effects in $TiSi_2$ and $CoSi_2$ films formed on n+ poly-Si will be analyzed.

High Current Conduction in $CoSi_2$ Films

High current tests under DC and pulsed stress conditions were carried out on the $CoSi_2$ films formed on n+ Si by high temperature rapid thermal process (RTP) (see Table 1). Comparison will only be made to the $TiSi_2$ (Ge-PAI) technology discussed in the last section.

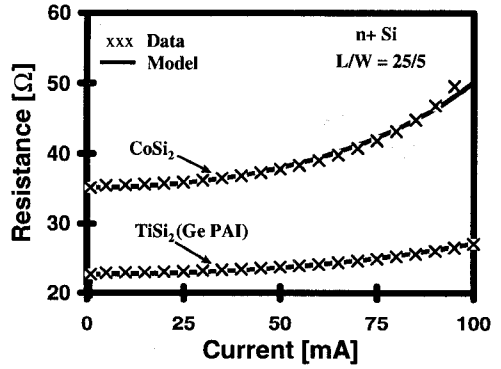


Fig. 9 High current behavior of $CoSi_2$ and $TiSi_2$ films under DC stress conditions along with the model developed in section 3.

Fig. 9 provides a comparison of high current conduction under DC stress conditions between $CoSi_2$ and $TiSi_2$ with L/W = 25/5. The high current model developed in the last section as (2) is shown to hold for the $CoSi_2$ film as well, though with a higher value of B (= 30 Ω/Watt) as compared to 16.5 Ω/Watt for the $TiSi_2$. B/R_0 is slightly bigger for $CoSi_2$ than $TiSi_2$ (0.853 per Watt Vs 0.728 per Watt). This is due to the slightly higher TCR of $CoSi_2$.

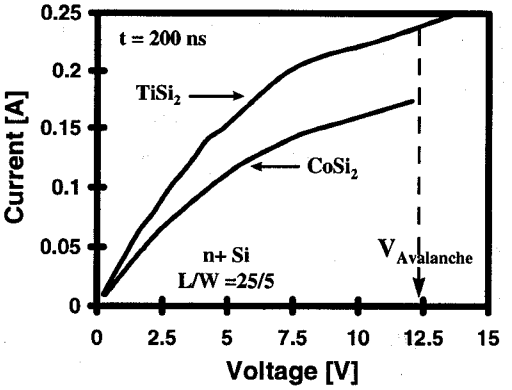


Fig. 10 Comparison of high current conduction between $CoSi_2$ and $TiSi_2$ films under a 200 ns pulsed stress condition.

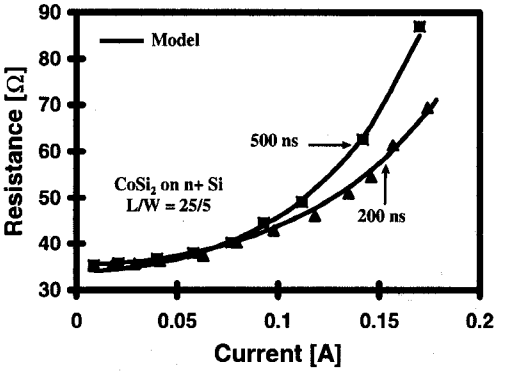


Fig. 11 High current conduction model for $CoSi_2$ films under pulsed stress conditions.

Fig. 10 shows the high current I-V curves (up to the avalanche voltage) for the $CoSi_2$ and $TiSi_2$ films under a 200 ns pulsed stress condition. In Fig. 11 (5) has been used to simulate high current conduction in the $CoSi_2$ film for two different pulse widths and the results are shown in good agreement with data. For the $CoSi_2$ film with L/W = 25/5, the values of λ were found to be 10.5 and 14.8 Ω/Watt for 200 ns and 500 ns pulse duration respectively.

Comparison of Mo Implant and Ge Pre-Amorphization Implant (PAI)

Fig. 12 compares the effect of using Mo implant with Ge-PAI before forming $TiSi_2$ films, on high current conduction under DC stress conditions. It can be observed that Mo implant makes the silicide resistance more strongly dependent on the current. This is verified by applying the model in (2) for L/W=10/2, which gives a slightly higher value for B/R_0 (= 2.485 per Watt) as compared to 2.317 per Watt for the $TiSi_2$

film with Ge-PAI. This result indicates that $TiSi_2$ films with Mo implant have a slightly higher TCR.

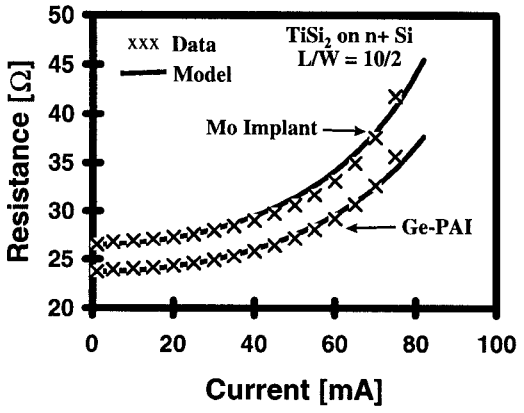


Fig. 12 High current conduction in $TiSi_2$ film under DC stress condition showing the effect of Mo implant.

The effect of Mo implant on the high current behavior under pulsed condition is also shown in Fig. 13, for L/W=25/5. The Mo implanted $TiSi_2$ film's resistance increases more rapidly with current giving a higher value for λ (=7.2 Ω/Watt), the parameter from the model in (5), as compared to 5.8 Ω/Watt for the Ge-PAI $TiSi_2$ film. Here R_0 is identical for the two cases. Again, the values of λ indicate that Mo implant results in a higher TCR.

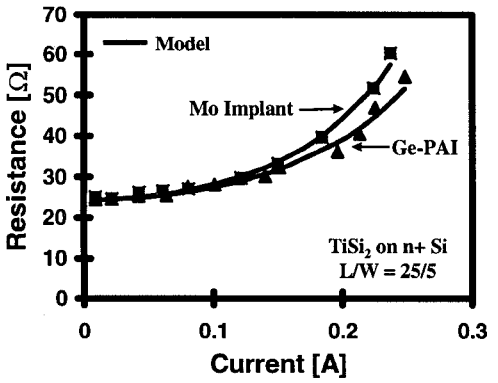


Fig. 13 Effect of Mo implant on the high current conduction under a 200 ns pulse showing a stronger dependence of film resistance on the current.

The higher TCR resulting in higher self-heating and the fact that Mo implanted $TiSi_2$ films have lower thermal stability [7] would make them more susceptible to high current degradation. This was found to be consistent with measured values of I_{crit} that were lower by up to ~ 25%.

High Current Effects in $TiSi_2$ and $CoSi_2$ Films on Poly-Si

The schematic representation of the test structure is shown in Fig. 14. The temperature coefficient of resistance (TCR) were measured to be 0.0025 ± 0.0002 and 0.0029 ± 0.0001 $^0C^{-1}$ for $TiSi_2$ and $CoSi_2$ films (formed on n+ poly-Si) respectively using low DC current. Fig. 15 shows the high current curves under DC stress conditions for $TiSi_2$ films on n+ poly-Si for two different geometries. Curves for $TiSi_2$ on n+ Si are also included for comparison. It can be observed that the films on poly-Si display larger sensitivity to current.

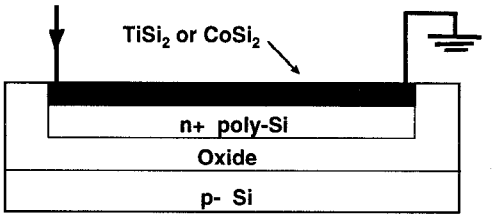


Fig. 14 Silicide structures on n+ poly-Si used in this study.

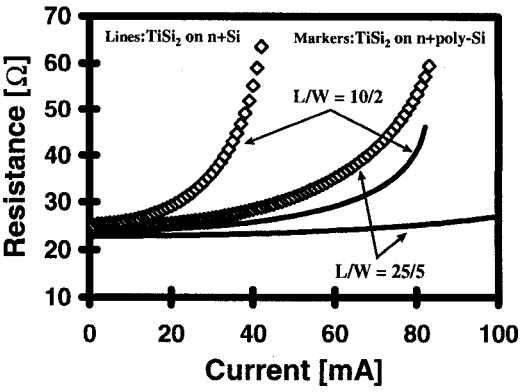


Fig. 15 High current conduction in $TiSi_2$ films on n+ poly-Si under DC stress displaying larger current sensitivity of resistance.

This is due to the higher thermal impedance of the oxide layer. Fig 16 shows the high current effects under DC stress conditions in $CoSi_2$ films on n+ poly-Si. Curves for the $TiSi_2$ films are also included for comparison. The $CoSi_2$ films display even larger sensitivity of resistance to current, as expected. The model from (2) is again shown to be valid and the values of B were found to be 85 and 345 Ω/Watt for the 25/5 and 10/2 $TiSi_2$ films respectively, and 148 and 610 Ω/Watt for the 25/5 and 10/2 $CoSi_2$ films respectively.

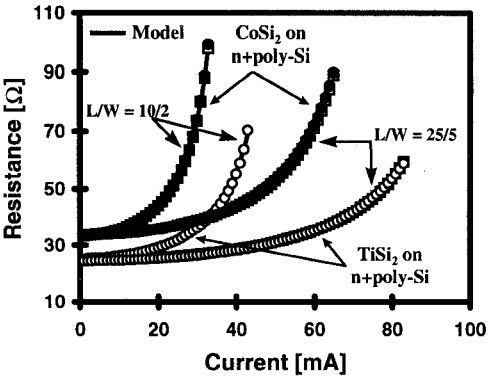


Fig. 16 Resistance sensitivity to current under DC stress is larger for $CoSi_2$ films, compared to that of $TiSi_2$, formed on n+ poly-Si.

The high current curves under pulsed stress conditions are shown in Fig. 17 for $TiSi_2$ and $CoSi_2$ films on n+ poly-Si. The

curves display characteristics similar to that of a silicide film on n+ Si (Fig. 6a). However, since there is no underlying junction, the resistance of the films continues to increase until the critical points. The snapback is believed to occur when the structure begins to melt.

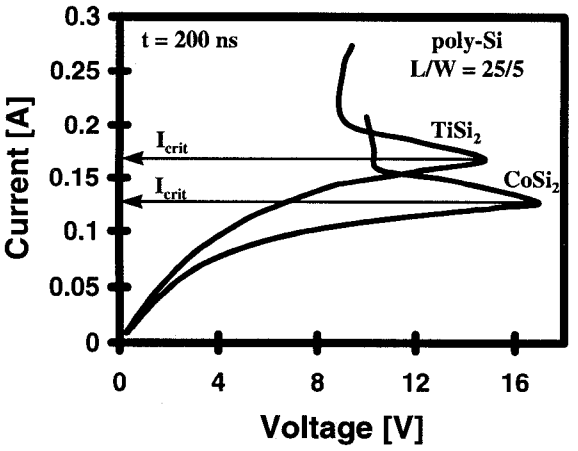


Fig. 17 The high current I-V curves for $TiSi_2$ and $CoSi_2$ films formed on n+ poly-Si under a 200 ns pulsed stress condition.

The failure currents are lower than that of silicides on n+ Si. These failure mechanisms will be discussed in detail in the next section. The high current model (5) under pulsed current is shown to be in excellent agreement with the data in Fig 18, all the way till snapback. The λ values, for a L/W=25/5 and pulse width of 200 ns, were found to be 18 Ω/Watt (or A^{-2}) and 38 Ω/Watt for the $TiSi_2$ and $CoSi_2$ films respectively. The higher λ compared to the n+ diffusion structures is due to the higher sheet resistance and lower thermal capacity of the poly-Si structures.

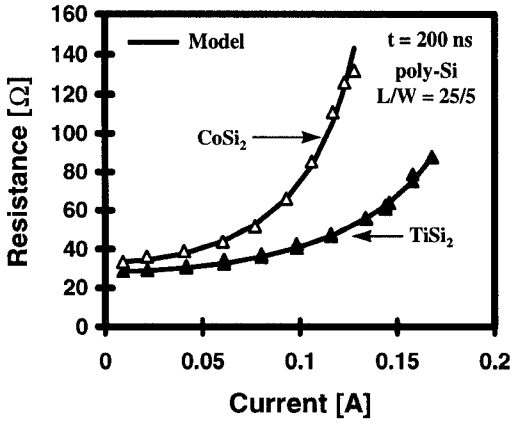


Fig. 18 High current conduction model under pulsed stress condition shown for $TiSi_2$ and $CoSi_2$ films on n+ poly-Si.

Finally, the effects of different salicide technology and processes on the high current behavior of thin silicide films are summarized in Fig. 19 for L/W=25/5. The parameter B, from the high current model under DC stress, in (2) and the parameter λ, from the high current model under pulsed stress, in (5) are shown to be good monitors of the impact of technology and process variations on the current dependence of resistance. The difference in the values of B for silicide films on n+ Si are mainly due to different sheet resistance and TCR. For silicide films on poly-Si the difference is mainly due to higher thermal impedance. Likewise, for silicide films on n+ Si, the difference in the values of λ are due to different sheet resistance and TCR, while for silicide films on poly-Si the difference is attributed to lower thermal capacity.

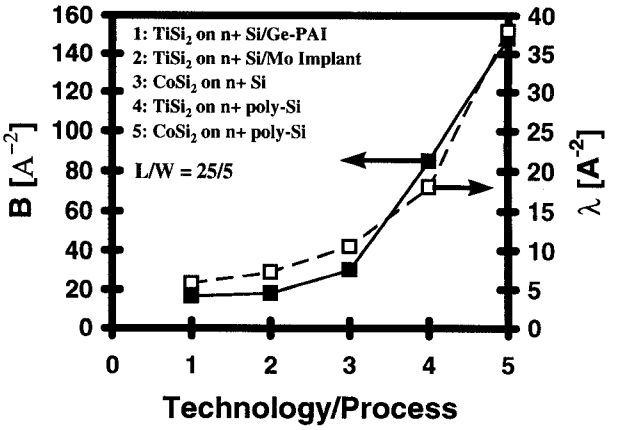


Fig. 19 Impact of salicide technology and process variations on the current sensitivity of resistance.

5. Failure Mechanisms

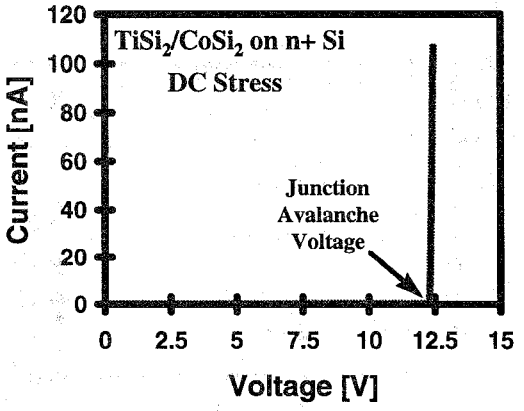
Failure Mechanisms of $TiSi_2$ and $CoSi_2$ films on n+ Si

For studying the failure mechanisms of silicide films under high current stress conditions, the pulsed technique provides more insight into the physics of degradation. The high current DC stress causes catastrophic failures, after which it becomes difficult to separate out one contributing factor from another. This section will therefore focus on deciphering the causes of silicide film degradation and failure under pulsed conditions.

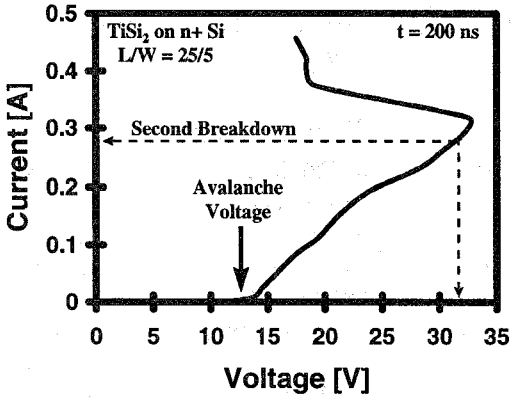
It was shown in Fig. 6a that in region CD, the voltage pulse increased linearly with time, up to a point at which the underlying p-n junction carried significant current by avalanche and the voltage pulse saturated. This is verified by stressing the p-n junction under the silicide structure with a DC voltage as shown in Fig 20a. Fig 20b shows the I-V characteristics of the junction under a 200 ns pulse stress. The junction avalanche voltage is in good agreement with that under DC stress (Fig. 20a). The voltage at the second breakdown point in Fig 20b is ~ 32 V which is nearly twice the second breakdown voltage in Fig. 6a. This is due to the voltage drop across the high resistance due to the current flow through the substrate.

Now, as the magnitude of the current pulse was increased beyond point D (in Fig. 6a), the instantaneous voltage pulse started to fall with time after rising sharply and the resistance of the post-stress silicide film increased irreversibly. This threshold point in the I-V curve was used to define I_{crit}. No electrical or physical degradation (from TEMs) was observed until this point which indicates that the non-linearity in the I-V characteristics under DC and pulsed stress conditions is due to self-heating of the silicide films.

In order to comprehend the real cause for the observed degradation, the post-stress breakdown voltage of the underlying p-n junction was monitored with each pulse of increasing magnitude. It was found that at point D, where the post-stress resistance of the $TiSi_2$ film begins to increase irreversibly, the avalanche voltage of the p-n junction begins to decrease slowly.



a)



b)

Fig. 20 *a) The reverse-bias DC I-V characteristics of the p-n junction showing avalanche voltage of ~ 12.5 V. b) The I-V characteristics of the p-n junction under a 200 ns pulse stress.*

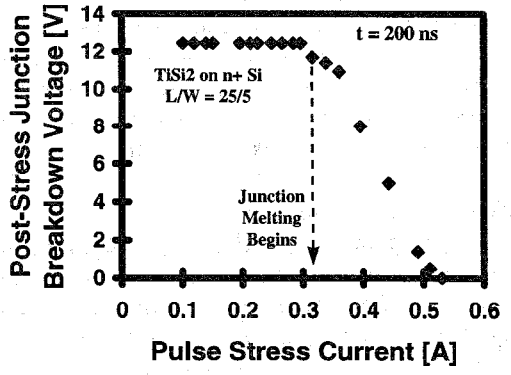


Fig. 21 *Junction avalanche voltage measured after each pulse of increasing amplitude decreases rapidly.*

This is shown in Fig. 21 for a $TiSi_2$ film on n+ Si stressed with 200 ns pulses. The decrease in the breakdown voltage indicates that Si in the junction region has melted and polycrystalline formation is responsible for the lower breakdown voltage. This point can also be termed as the "second breakdown" point, since there is an irreversible change in the junction characteristics. The junction heating now causes the silicide to begin to melt and degrade due to morphological changes after re-solidification, causing an irreversible increase in the resistance of the structure.

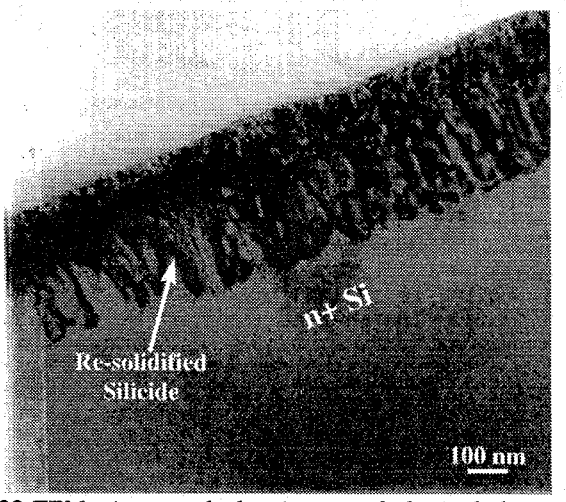


Fig. 22 *TEM micrograph showing morphological change in a silicide film upon re-solidification after being stressed past the critical point by a 200 ns pulse.*

Fig 22 shows a TEM micrograph of a degraded silicide layer with distinct morphological changes. Fig. 23 shows the post-stress resistance rise of the L/W=25/5, $TiSi_2$ and $CoSi_2$ films monitored with a low stress DC measurement after each pulse of increasing magnitude. The critical current for both types of silicide are indicated with vertical arrows. These are points at which the resistance of the films begins to increase.

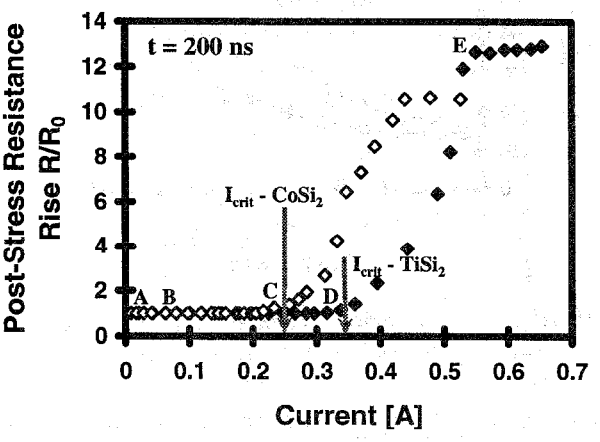
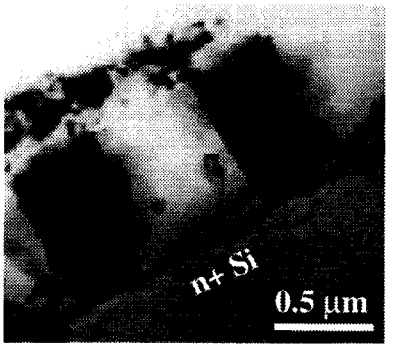
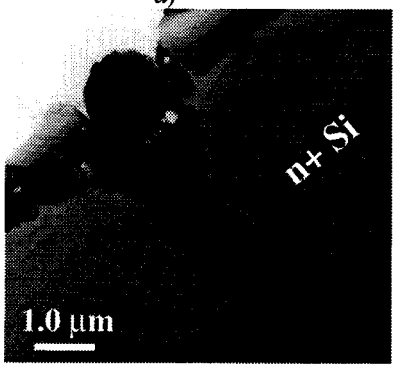


Fig. 23 *The post-pulse resistance rise for $TiSi_2$ (solid markers) and $CoSi_2$ (empty markers) films formed on n+ Si under a 200 ns pulsed stress condition. The letters indicate the various regions in the high current curve from Fig. 6a for the $TiSi_2$ film.*

The irreversible change in the silicide resistance is introduced due to thermal effects resulting from second breakdown [10-11] in the underlying diffusion region. This effect is introduced by current localization due to the negative resistance coefficient of Si beyond a critical temperature. This causes the silicide film to melt at hot spots. Since the melting point of $CoSi_2$ (~1326 ^{0}C) is lower than that of $TiSi_2$ (~1500 ^{0}C) [12], and that $CoSi_2$ has higher resistivity than $TiSi_2$, the $CoSi_2$ film degrades at a lower current. Beyond point E, the junction is spiked by the contact as shown by the TEM in Fig. 24. The saturation point in Fig. 23 (for $TiSi_2$) agrees well with the junction short point in Fig. 21. When the contact spike reaches the junction, R/R_0 saturates as shown in Fig. 23. The current now flows from one contact to another through the p substrate in parallel with the degraded silicide. The resistance in that region is greater than 10(12) times the initial resistance of the $CoSi_2$($TiSi_2$) film. This indicates that the sheet resistance of the new material is ~10(12) times higher than that of the silicides and is in rough agreement with that of a poly-Si film. This poly-Si film eventually fails like a fuse as current is increased further.



a)

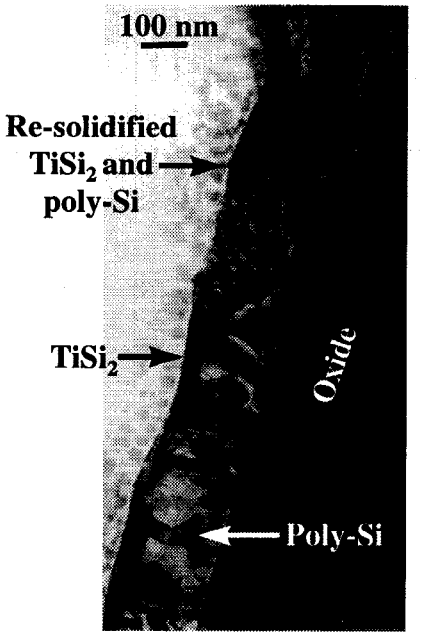


b)

Fig. 24 TEM micrographs showing a) virgin contacts and b) damaged contact spike into the substrate.

Failure Mechanisms of $TiSi_2$ and $CoSi_2$ films on n+ poly-Si

Silicide films formed on n+ poly-Si degrade at lower current levels as pointed out in section 4, due to the higher thermal resistances of these structures. The post-stress resistance rise in these films after the critical (snapback) points in the high current I-V characteristics (Fig. 17), follow the behavior of silicide films on n+ Si, shown in Fig. 23. That is, the film resistance saturates to a value (~12 times that of the unstressed film) before failing like a fuse. The resistance rise is again associated with morphological changes in the film upon re-solidification after melting during the high current pulsing. This is shown by a TEM micrograph in Fig. 25. The micrograph clearly shows a section of the film that is still intact and a section that has undergone morphological changes.



Fig, 25 TEM micrograph showing a $TiSi_2$ film on n+ poly-Si showing a section that has undergone morphological changes upon re-solidification.

Geometry and Pulse Width Dependence of I_{crit}

The dependence of the critical current on the geometry of the films and pulse width can be modeled as follows. Since, it has been shown that the silicide films reach melt temperatures, the energy, E, required to melt a film of length L and width W can be expressed as,

$$E = a(W \cdot L) \tag{6}$$

where a is a proportionality constant. The energy for a pulse of amplitude I_{crit}, and duration t, can be expressed as,

$$E_{crit} = I_{crit}^2 \cdot R \cdot t = b \cdot \left(\frac{L}{W}\right) \cdot I_{crit}^2 \cdot t \tag{7}$$

Here b is a proportionality constant. From (6) and (7), we get, under adiabatic assumption,

$$I_{crit} = K \cdot \frac{W}{\sqrt{t}} \tag{8}$$

where K depends on the material properties and the thickness of the silicide. I_{crit} is shown to be linearly dependent on W for different silicides in Fig. 26. It can also be observed that the $CoSi_2$ films have lower I_{crit} compared to $TiSi_2$ films and poly-Si lowers these values even further. The pulse width dependence of I_{crit} is shown in Fig. 27 for $TiSi_2$ and $CoSi_2$ films on poly-Si. The adiabatic model from (8) is shown to be in good agreement with the data. Note that the model in (8) will be less accurate for silicide films on Si, due to heat diffusion into the substrate.

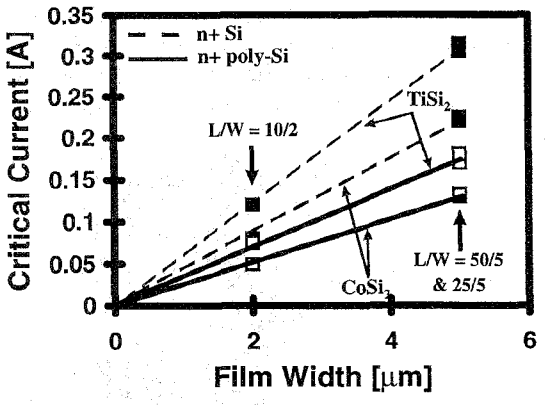


Fig. 26 Proportionality of I_{crit} to the film width, W, shown for $TiSi_2$ and $CoSi_2$ films on n+ Si and n+ poly-Si. The pulse duration was 200 ns.

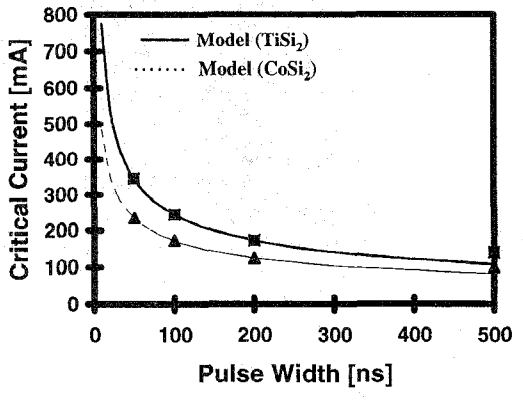


Fig. 27 Pulse width dependence of I_{crit} for L/W = 25/5, $TiSi_2$ and $CoSi_2$ films on n+ poly-Si. The model is based on (8).

6. Conclusions

In conclusion we have characterized and modeled the high current behavior of thin $TiSi_2$ and $CoSi_2$ films used in advanced CMOS technologies. High current conduction in silicides have been shown to be strongly affected by the technology and process conditions. The non-linear resistance rise of silicide films under DC and pulsed high current stress has been shown to be due to self-heating. Two physical parameters, B and λ, associated with DC and pulsed current stress, have been shown to be able to describe the sensitivity of the films to high current conduction. At high current an abrupt lowering of the resistance of silicided diffusions has been observed that can be important in the operation of advanced ESD/EOS and I/O buffer circuits. The sudden resistance drop in these structures under high current stress has been shown to be related to melting of the silicide structures. The critical current for this irreversible degradation has been shown to be determined by the silicide film width and the time duration of the pulse. Further, we have also shown that the $CoSi_2$ films and silicides on poly-Si have a lower failure threshold under high current stress conditions. Extensive microstructure characterization of the silicide films using TEM has been performed to comprehend the evolution of silicide film degradation under high current stress. Thus, an understanding of these high current effects has been developed along with the physics of the failure mechanisms which will enable the impact of technology design and scaling of silicide films to be defined for the reliability of deep sub-micron CMOS technologies.

Acknowledgments

This research was supported by Texas Instruments Inc. Authors would like to gratefully acknowledge Dr. William Hunter and Dr. Ping Yang (now with TSMC) of TI, for their support and encouragement. Thanks to Dr. Vince McNeil and Dr. Terence Breedijk for technical discussion on the processing issues. They would also like to acknowledge Michael Coviello for the TEMs and Mike Obrien for excellent technical assistance during the experiments.

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