A Body-Contact SOI MOSFET Model for Circuit Simulation

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Introduction: Making contact to the body of a partially depleted (PD) SOI transistor offers another degree of design freedom. For example, DTMOS [1] has demonstrated that the body-contact can be used to enhance the power/delay performance. It has also been shown that the body-contact plays important role in eliminating the floating-body instability [2] for sensitive circuits. A complete SPICE model that explicitly addresses the non-idealities of the body-contact is surely needed for SOI circuit design. Here we present a compact body-contact SOI MOSFET model that has been implemented in BSIMPD2.0 [3] for circuit simulation.

Model: The model can be described using a transistor with the T-gate layout shown in Figure 1. The body-contact provides the transistor a resistive path for charging/discharging of the body. However the associated body-contact diffusion and the "Extended-Gate" region interact with other electrical terminals as well and may be represented by the equivalent circuit shown in Figure 2. The lumped resistance between B node and BC node consists of the intrinsic body resistance $R_b$ and the extrinsic body resistance $R_{bc}$. $R_b$ is modeled by $R_{body} \cdot W/L$, where $R_{body}$ is the body sheet resistance along the channel width. $R_{bc}$ is modeled by $R_{sh} \cdot N_{sh}$, where $R_{sh}$ and $N_{sh}$ are the body sheet resistance and the number of squares in the "Extended-Gate" region, respectively.

The parasitic diodes between B and S/D are characterized by the parameters $P_{sh}, P_{sh}$, the perimeter length of body-contact at the sides of source/drain. Similarly, the parasitic capacitances between B and G/E are characterized by the parameters $C_{sh}, C_{sh}$, which stand for the gate/substrate-to-body overlap. Since these parameters are layout-dependent, they are specified in a per-instance manner. According to the layout geometry of Figure 1, we have $P_{sh}=PLS, P_{sh}=PLD, A_{sh}=PWB, PLC$ and $A_{sh}=(PWB+PLC)$.

Due to the distributed nature of $R_b$, a lumped resistor is no longer satisfactory for sensitive circuits. Therefore, an accessible B node is provided in BSIMPD so that users can perform distributed simulation by partitioning a wide transistor and cascading the body resistors of the sub-transistors (Figure 3). For each sub-transistor, the partition number, $N_{sh}$, should be specified so that the transistor current and charge can be scaled by $N_{sh}$ without over-estimating the narrow-width effect. Note that the width can be non-uniformly partitioned as long as the sum rule $\sum N_{sh}^2 = 1$ is fulfilled.

Impact on Device Parameters: The importance of body-contact model can be demonstrated from another perspective: Since most of the model parameters of floating-body transistors have to be extracted from body-contact devices, the non-ideal body-contact effect needs to be taken into account in parameter extraction. Its impact on the key device parameters in the high body-bias regime, which is essential to PD SOI operations, is investigated using a typical body-contact device with $W=5\mu m, L_{sh}=0.1\mu m$.

Figures 4 and 5 shows that the drain current at high $V_b$s is much lower than what the ideal body-contact simulation predicts (steep increase). It is mainly due to the IR drop of body potential caused by the forward-biased diode current flowing through the distributed body resistance. Since the diode current increases with temperature, the discrepancy becomes larger at 140°C. It can be seen that the simulation result agrees very well with the measurement data after considering the non-ideal body-contact effect.

Figure 6 and 7 shows the correction of the threshold voltage in the high body-bias regime made by the non-ideal body-contact model. As expected, the threshold voltage drops much more slowly and smoothly in the non-ideal case. This implies that the ideal body-contact assumption in parameter extraction may lead to a wrong body-effect ($V_t$ as a function of $V_b$s) prediction, which is crucial to the noise margin of the pass-gate and dynamic logic design.

Impact on Performance Prediction: Figure 8 shows the impact of the non-ideal body-contact effect on the transistor switching speed. Due to the parasitic capacitances caused by $A_{sh}, C_{sh}$, and the extra junction charges induced by $P_{sh}, C_{sh}$, the speed performance of an inverter gate is approximately degraded by 30% in this case.

Conclusion: Since the body-contact is widely used in not only critical circuit design but also test structures for parameter extraction, a compact SOI body-contact model which can accurately capture the body potential, is crucial to the accuracy of circuit simulation. A body-contact model, including layout-dependent parasitic diodes and capacitances, as well as an accessible body node for high-precision segmented-transistor simulation, has been developed and implemented in BSIMPD2.0. The impact of the non-ideal body-contact effect on the device parametrics and performance are also investigated based on this model.
Fig. 1. A T-gate layout used to illustrate the body-contact model. The layout geometry determines all the instance parameters representing the non-idealities of the body-contact.

Fig. 2. The equivalent circuit used in BSIMPD to model the non-ideal body contact. G: gate, E: substrate, S: source, D: drain, B: body, BC: body-contact. The diodes between B and S/D are the gated diodes at the sides of source/drain (in Figure 1 where "Extended-Gate" and "Source" / "Drain" intersect). The capacitance between G and B is the gate-to-body overlap capacitance in the "Extended-Gate" region. The capacitance between E and B is the substrate-to-body overlap capacitance in both the "Body-Contact" and the "Extended-Gate" region.

Fig. 3. An accessible B node is provided in BSIMPD to facilitate the distributed simulation.

Fig. 4. Idsat (Ids @ Vgs=Vdd, Vds=0.05V) versus Vbs showing the importance of body-contact model in the high body-bias regime.

Fig. 5. Idsat (Ids @ Vgs=Vdd, Vds=Vdd) versus Vbs showing the significant threshold voltage roll-off in the high body-bias regime without considering the non-ideal body-contact effect.

Fig. 6. Vth (Vth @ Vgs=Vdd, Vds=0.05V) versus Vbs showing the significant threshold voltage roll-off in the high body-bias regime without considering the non-ideal body-contact effect.

Fig. 7. Vsat (Vt @ Vgs=Vdd, Vds=Vdd) versus Vbs showing the significant threshold voltage roll-off in the high body-bias regime without considering the non-ideal body-contact effect.

Fig. 8. The output waveforms of an unloaded 51-stage ring oscillator showing the optimistic performance-prediction made by the ideal body-contact assumption. The error of switching speed is around 30% in this case.

References

[3] Available at www-device.eecs.berkeley.edu/~bsim3soi