BSIMP: A Partial-Depletion SOI MOSFET Model for Deep-Submicron CMOS Designs

Pin Su, Samuel K. H. Fung*, Stephen Tang, Fariborz Assaderaghi* and Chenming Hu

Department of EECS, University of California at Berkeley, Berkeley, CA 94720
*IBM Semiconductor Research and Development Center, Hopewell Junction, NY 12533

Abstract
BSIMP: A physics-based SPICE model is developed for bridging deep-submicron CMOS designs using partially-depleted SOI technologies. Formulated on top of the industry-standard bulk-MOSFET model BSIM3v3 for a sound base of scalability and robustness, BSIMP captures SOI-specific dynamic behaviors with its built-in floating-body, self-heating and body-contact models. A parameter-extraction strategy is demonstrated, and the simulation efficiency is studied. The model has been tested extensively within IBM on state-of-the-art high speed SOI technologies. It has been implemented in many circuit simulators.

Introduction
Four technological trends set the stage for partially-depleted SOI (PDSOI) to become an important IC technology for the 21st century: (1) High performance. PDSOI provides a performance gain of 20 to 35 percent over bulk CMOS [1] due to the reduction of junction capacitance and the absence of the body-bias effect in series connected devices, e.g. in NAND and NOR gates. (2) Low power. With the same performance SOI can operate at a lower voltage and therefore lower power. (3) Mixed Technologies. SOI provides a way to isolate analog circuits from substrate noise and provides high-Q inductors. It may be useful to embedded DRAM because of good signal isolation from the logic circuit blocks. (4) Process simplicity. SOI may reduce some future bulk-technology’s manufacturing difficulties such as isolation, shallow junction, and latchup sensitivity.

As PDSOI technology becomes more widely used, a robust and physically accurate SPICE model is sorely needed to reduce the risk of inadequate circuit designs. BSIMP (Berkeley Short-Channel IGFET Model - Partial Depletion) attempts to serve as this critical communication vehicle between IC design and manufacturing.

BSIMP is jointly developed by University of California at Berkeley and IBM, and its source code may be downloaded from the web [2]. This model is a derivative of the industry-standard bulk-MOSFET model BSIM3v3 [3]. Three important additions are made to the SOI model: floating-body model, self-heating model and body-contact model.

Floating-body Model
To accurately model the potential of the floating body, which has strong impact on the device behavior, the circuit shown in Figure 1 is solved for the body voltage. In DC, this voltage is determined by the various body current components. For AC/ transient simulation, the displacement currents originating from capacitive couplings will also contribute. Once the body potential is found, the impact of the floating body on I_D can be captured through an accurate threshold voltage model in the high forward body-bias regime.

A. DC Model
The IV characteristics in Figure 2 show kinks in the high drain-bias regime due to the rise in body voltage that is caused by the impact-ionization current (I_n). The excess I_D is a major source of performance gain of SOI over bulk and thus needs to be well modeled. Since the steady-state body potential is determined by the counter-balance of I_n and the body-source diode current, accurate I_n and diode current models, which takes into account the tunneling effect in the high-field halo (pocket implant) region of the junctions, are developed to achieve the accuracy of the BSIMP model.

B. AC/Transient Model
During switching, the body potential is determined by the initial state of the body charge as well as the body-to-gate/drain/source/backgate capacitive coupling. This results in the history dependence of gate delay shown in Figure 3. To catch this delay variation, an accurate modeling of the capacitances and the body time constant is required. As shown in Figure 4, the model-prediction of the body potential for fast gate/drain voltage ramp shows good agreement with 2D device simulation. As the gate oxide thickness is scaled down, the impact of quantum effects on the gate capacitance becomes significant. A charge-thickness model (CTM) [4], which considers the quantization of inversion charges and poly-gate depletion in the capacitance model, is embedded in BSIMP to support deep-submicron CMOS designs.

The pass-gate leakage shown in Figure 5 is another consequence of the floating-body effect and can cause circuit failures. Since V_{th} can be very high during a fast pull-down of the source voltage, a significant lateral bipolar current develops and gives rise to the leakage current. Therefore, an accurate bipolar current model that accounts for the decrease of bipolar gain due to high level injection is important to pass-gate circuit simulation.
Self-heating Model

Self-heating may reduce the body potential by inducing more diode leakage and thus degrade the current drive beyond the usual bulk-MOSFET temperature sensitivity. An auxiliary $R_4C_4$ circuit (Figure 6) is employed to calculate the device temperature. In a circuit, the power dissipation is low and the switching period is usually much shorter than the thermal time constant. Therefore the self-heating effect is generally insignificant. Self-heating free IV characteristics may be deduced from the measured IV data if $R_a$ is known. $R_a$ can be extracted from a high-frequency AC output impedance measurement [5].

Body-contact Model

Since the body-contact (BC) is widely used in critical circuits (e.g., PLL and other analog circuits), an accurate model that can represent the non-idealities (e.g., distributed body resistance) of the contact is essential to precision-oriented simulations. Based on the T-gate layout shown in Figure 7, the geometry-dependent parasitic diodes and capacitances, as well as an accessible body node for building segmented-transistor models are incorporated in BSIMPD. This BC model is of equal importance to the floating-body model. It affects not only circuit simulation but also model parameter extraction because most model parameters are extracted from BC test structures (Figure 8). Ignoring the BC effect in parameter extraction may lead to inaccurate body-effect parameters, with severe consequences to the noise margin calculation of the pass-gate and dynamic logic design [6].

Parameter-Extraction Strategy

Figure 9 shows a proposed parameter-extraction flow of BSIMPD. Elimination of self-heating effect from measured IV data of body-contact devices is first performed. This can be achieved by the extraction of $R_a$ and the determination of the temperature dependency of major device parameters such as carrier mobility and threshold voltage. Once self-heating free IV characteristics are obtained, the basic MOSFET parameters can be extracted following procedures similar to bulk transistor modeling. The forward body-bias regime, however, should be emphasized due to the floating-body operation. The drain and therefore the body voltage may be particularly high during the burn-in test.

After the parameters of various body current components (i.e., $I_b$, diode, gate-induced-drain-leakage and bipolar currents) are directly extracted from body-contact devices, verification with floating-body IV characteristics and global optimization should be carried out to ensure accuracy.

Simulation Efficiency

To investigate the simulation efficiency of BSIMPD, two benchmark circuits: a 8-bit decoder and a 51-stage ring oscillator are employed to assess the model performance in DC and transient operation, respectively. As shown in Figure 10, the run-time statistics obtained from Berkeley SPICE3f4 are normalized based on the results of BSIM3v3 bulk model. The ~1.5X total iteration number (convergence) of BSIMPD originates from the stiff nature of the long floating-body time constant. While the ~2X load time per iteration (complexity) of BSIMPD is mainly due to the complex equations (e.g., exponential function) utilized in modeling the various body current components. The overall load time (efficiency) of the floating-body simulation is around 3X compared with the bulk BSIM3v3 model.

Summary

A physics-based partially-depleted SOI MOSFET model has been developed to support deep-submicron CMOS designs for SOI technologies of the 21st century. Based on the industry-standard BSIM3v3 bulk model, BSIMPD models the PDSOI-specific floating-body, self-heating and body-contact effects. This model is able to capture the various dynamic behaviors in the PDSOI circuitry by the floating-body simulation.

BSIMPD has been tested extensively within IBM on state-of-the-art high speed SOI technologies [7]. This model has been implemented in Berkeley SPICE3f4 as well as many commercial circuit simulators such as HSPICE, SPECTRE, SmartSPICE, ELDO (being implemented) and so on.

Acknowledgement

This research is supported by National Science Foundation under Contract ECS-9634217 and the MICRO program. P. Su would like to acknowledge the help he received from Drs. D. Sinitsky, W. Liu, J. Feng and W. Jin during this work.

References

[2] www-device.eecs.berkeley.edu/~bsimsoi
Fig. 1. Circuit representation of the BSIMPD model of the floating-body voltage. Body voltage is a function of body charge, which is determined by various body currents and displacement currents.

Fig. 2. BSIMPD accurately models the IV characteristics of a PDSOI transistor showing excess current drive due to floating-body kink effect.

Fig. 3. Delay per stage of a PDSOI unloaded inverter chain shows a history dependence due to dynamic variations of the stored body charges and thus variation of $V_{TH}$.

Fig. 4. The body potential predicted by BSIMPD for fast gate/drain voltage ramp agrees well with 2D device simulation.

Fig. 5. Peak leakage current of a pnp gate transistor following a fast pull down of the source voltage demonstrates another floating body effect, which is captured by BSIMPD.
Fig. 6. BSIMPD uses this self-heating equivalent circuit driven by the transistor power to model the device temperature (node-voltage of T).

Fig. 7. Layout representation illustrating the body-contact model of BSIMPD. Distributed body resistance as well as geometry-dependent parasitic source/drain diodes, gate-to-body (gray area) and body-to-backgate (hashed area) overlap capacitances are considered.

Fig. 8. Layout of the H-gate body-contact test structure used in model-parameter extraction.

Fig. 9. Parameter extraction flow of BSIMPD.

Fig. 10. Comparison of simulation efficiency between BSIMPD and BSIM3v3 performed by Berkeley SPICE3f4.