New Paradigm of Predictive MOSFET and Interconnect Modeling for Early Circuit Simulation

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Abstract
A new paradigm of predictive MOSFET and interconnect modeling is introduced. This approach is developed to specifically address SPICE compatible parameters for future technology generations. For a given technology node, designers can use default values or directly input $L_{eff}$, $T_{ox}$, $V_t$, $R_{on}$ and interconnect dimensions to instantly obtain a BSIM3v3 customized model for early stages of circuit design and research. Models for 0.18µm and 0.13µm technology nodes with $L_{eff}$ down to 70nm are currently available on the web. Comparisons with published data and 2D simulations are used to verify this predictive technology model.

Introduction
The pace of MOSFET technology scaling and new product development has accelerated in recent years and shows no sign of slowing down [1]. Competitive circuit design and research must often begin before a future generation of MOSFET technology is fully developed. In that case, a reasonably accurate predictive SPICE model that can be conveniently customized would be very useful.

Such a customizable model is presented here. It is based on several facts: First, for a given technology node, the device design and process technologies used throughout the semiconductor industry do not vary a lot. Even though the largest source-drain current $I_{ds}$ may vary significantly from one company’s technology to another, there is a commonality in the general behavior of the devices. Second, the salient differences in $I_{on}$ and gate capacitance, etc. are due to variation in $L_{gate}$, $L_{eff}$, $T_{ox}$, $V_t$, $R_{on}$ (source-drain series resistance per square area) and $V_{ds}$. Among these, circuit designers already treat $L_{gate}$ and $V_{ds}$ as design variables. We will refer to $L_{eff}$, $T_{ox}$, $V_t$, and $R_{on}$ as the process parameters. Third, the industry standard compact model BSIM3v3 is grounded in devices physics and has sufficient predictiveness to accommodate the range of process parameters encountered in a single technology node [2]. For example, if a circuit designer specified a new $T_{ox}$, not only $I_{ds}$, but also the leakage current $I_{off}$, output conductance, body effect, etc. will be correctly modeled. So the remaining challenge is to obtain a typical or benchmark BSIM3v3 model (a list of over 100 parameters for modeling currents and device capacitance) and an interconnect capacitance and inductance model for each technology node.

In this paper a general methodology for predicting these parameters is presented. Comparisons between published data and model predicted data are used to verify the validity of this approach. As the demonstrations, this predictive technology model is applied to simulate typical device and interconnect delays for several technology nodes and used to design a one bit full adder.

Predictive Methodology
Fig. 1 shows the methodology of generating a benchmark model for a given technology node.

![Technology Parameters](image)

- Arrive at expert consensus for typical values and ranges of $L_{eff}$, $T_{ox}$, $V_t$, $R_{on}$, $X_j$ and dimensions of interconnect.

![BSIM3v3 DC and AC Parameters](image)

- Use typical process parameters: $L_{eff}$, $T_{ox}$, $V_t$, $R_{on}$, $X_j$
- Calculate physical parameters: $N_{cb}$, $K1$
- Extract secondary parameters from 2D simulations or research devices
  - DC: $N_{sb}$, $N_{sw}$, $N_{sw}$
  - AC: $C_{gs}$, $C_{gs}$, $C_{gd}$, $C_{gs}$, $C_{gs}$, $C_{gs}$, $C_{gs}$, $C_{gs}$, $C_{gs}$, $C_{gs}$, $C_{gs}$, $C_{gs}$, $C_{gs}$
- The remaining parameters are taken from the last generation of technology unchanged.

![Interconnect Capacitance/Inductance Parameters](image)

- Perform Raphael™ simulation for a range of interconnect dimensions
- Generate center values: $C_{ib}$, $C_{ic}$, $L_0$, $k_1$, and $R$
- Extract first order, second order and cross-product coefficients for local, intermediate and global interconnects:
  - $C_{ib}$, $C_{ic}$, $C_{ib}$, $C_{ic}$, $C_{ib}$, $C_{ic}$, $C_{ib}$, $C_{ic}$, $C_{ib}$, $C_{ic}$, $C_{ib}$, $C_{ic}$, $C_{ib}$, $C_{ic}$

![Verification](image)

- Comparisons with available data
  - Inputs: $L_{eff}$, $T_{ox}$, $V_t$, $R_{on}$
  - Outputs: $I_{on}$, $I_{off}$, $g_m$, $S$, $V$, $C$
- Feedback from IC companies

Figure 1: Methodology of generating a predictive benchmark model
From the previous work, it has been determined that the proper categorization of BSIM3v3 parameters based on their physical meaning and model sensitivity is crucial for efficient prediction [3, 4]. We address this issue as Fig 1 shows. First, the typical values and ranges of the process parameters and interconnect metal and dielectric dimensions are determined by a survey of the literature including the National Technology Roadmap for Semiconductors [NTRS] as well as informal discussions with industry researchers. These processing and electrical characteristics represent our perspective on that future technology node and will serve as the default values in the following steps. Second, a group of 20 secondary parameters (secondary to the process parameters) are extracted from the DC drive current and AC capacitance characteristics generated by commercial 2D devices and simulated and confirmed with measurements on early research devices. The remaining 80 BSIM3v3 parameters are taken from a previous well-characterized generation of technology. The new approach may be more accurate because it can capture information such as subtle effects of doping profiles that 2D simulation and early research device may miss.

For interconnect, two distinctive types of metal layout are studied as shown in Fig 2 and Fig 3. In the coupled line case, top layer is considered separately because of its absence of top ground layer.

![Fig 2: Single line structure for extracting capacitance/inductance](image)

![Fig 3: Coupling lines structure for extracting capacitance/inductance. Right is the top layer with packaging materials covered.](image)

The interconnect resistance, capacitance and inductance are simulated with commercial simulators over the range of metal sizes and spaces, inter-layer-dielectric (ILD) and inter-metal-dielectric (IMD) dimensions, and ILD/IMD dielectric constants ($k_{ILD}/k_{IMD}$). The simulated capacitances and inductances are captured with twelve equations (line-to-ground/line-to-line capacitances and self/mutual inductances for local, intermediate and global interconnects) that are second order Taylor expansions of the dimensions and dielectric constants. This analytical approach has the following form:

$$F = F_0 + F_1 \cdot \Delta w + F_2 \cdot \Delta t + F_3 \cdot \Delta h + F_4 \cdot \Delta s + F_{ILD} \cdot \Delta k_{ILD} + F_{IMD} \cdot \Delta k_{IMD}$$

$F$ stands for either capacitance or inductance, with different coefficients extracted. $F_0$ is the center value for the typical interconnect dimensions. $\Delta$ term is the difference between the customized value and our typical one (e.g. $\Delta w = w - w_0$) and the other $F_i$'s are the corresponding coefficients. This simple form provides excellent computational efficiency while maintaining accuracy.

Finally, the prediction and customization capability is verified by comparison with the available data in the literature [4-12] and by feedback from interested companies.

### Results and Evaluation

Two benchmark models have been developed from this methodology and are available on the web at http://www-device.eecs.berkeley.edu/~ptm. They are intended for 0.18μm ($L = 0.08-0.15\mu$m, $T_{ox} = 3.5-5$nm) and 0.13μm ($L = 0.07-0.10\mu$m, $T_{ox} = 2.5-4$nm) nodes. Table 1 compares the predicted $I_{on}$ and $I_{off}$ with measured data for a number of published technologies.

<table>
<thead>
<tr>
<th>$L_{on}$</th>
<th>$V_{dd}$</th>
<th>$T_{ox}$</th>
<th>$R_{on}$</th>
<th>$I_{on}$</th>
<th>$I_{off}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit</td>
<td>μm</td>
<td>V</td>
<td>nm</td>
<td>Ω/s</td>
<td>μA/μm</td>
</tr>
<tr>
<td>Range</td>
<td>0.05-0.10</td>
<td>1.8-2.5</td>
<td>0.2-0.4</td>
<td>50-600</td>
<td>Pub.</td>
</tr>
<tr>
<td>0.12μm</td>
<td>0.05[2]</td>
<td>1.5</td>
<td>3</td>
<td>0.3</td>
<td>250</td>
</tr>
<tr>
<td>NMOS</td>
<td>0.10[2]</td>
<td>1.5</td>
<td>3.6</td>
<td>0.35</td>
<td>70</td>
</tr>
<tr>
<td>0.13μm</td>
<td>0.10[1]</td>
<td>1.5</td>
<td>3.6</td>
<td>0.27</td>
<td>220</td>
</tr>
<tr>
<td>PMOS</td>
<td>0.09[1]</td>
<td>1.5</td>
<td>3.3</td>
<td>0.25</td>
<td>400</td>
</tr>
<tr>
<td>Range</td>
<td>0.05-0.15</td>
<td>1.2-3.5</td>
<td>0.2-0.5</td>
<td>50-600</td>
<td>Pub.</td>
</tr>
<tr>
<td>0.18μm</td>
<td>0.10[1]</td>
<td>1.8</td>
<td>4.5</td>
<td>0.28</td>
<td>250</td>
</tr>
<tr>
<td>NMOS</td>
<td>0.08[1]</td>
<td>1.8</td>
<td>3.8</td>
<td>0.25</td>
<td>250</td>
</tr>
<tr>
<td>0.12[1]</td>
<td>1.8</td>
<td>4.5</td>
<td>0.42</td>
<td>250</td>
<td>455</td>
</tr>
<tr>
<td>0.18μm</td>
<td>0.12[1]</td>
<td>1.5</td>
<td>4.2</td>
<td>0.25</td>
<td>500</td>
</tr>
<tr>
<td>PMOS</td>
<td>0.11[1]</td>
<td>1.8</td>
<td>3.9</td>
<td>0.1</td>
<td>500</td>
</tr>
<tr>
<td>0.15[1]</td>
<td>1.8</td>
<td>4.5</td>
<td>0.3</td>
<td>500</td>
<td>240</td>
</tr>
</tbody>
</table>
In Table 1, the process parameters, i.e., $L_{\text{eff}}$, $T_{\text{ox}}$, $V_t$, and $R_{\text{ds}}$, are applied as input. Their values are replaced by published data, or remain as the default values when they are not available. Even though the different technologies cover a wide range of variations in $L_{\text{eff}}$, $T_{\text{ox}}$ and $V_t$, the predicted data matches published data very well. In general, the $I_{\text{on}}$ error is within about 10%.

Actually, much beyond the $I_{\text{on}}$ and $L_{\text{off}}$, the full device characteristics could be predicted with the benchmarked BSIM3v3 parameters. Fig. 4 reports the agreement between the customized benchmark models with three published technologies. For both DC on state/sub threshold current and AC gate capacitance, excellent agreement is achieved for the full voltage range.

In Fig. 5, the analytical interconnect capacitance and inductance models are verified with the simulated results. For wide ranges of metal dimensions, the models agree with simulation within 15% error. With this analytical model, the designers could calculate out the interconnect capacitance and inductance reasonably accurately in a very short time.

**Figure 5: Error map of interconnect models relative to 2D simulations**

**Demonstrations for Early Circuit Design**

The predictive models developed in this work provide designers with a convenient and accurate way to start their advanced circuit research in parallel with process technology development. As application examples, we apply the models to evaluate typical device and interconnect delays for 0.18μm and 0.13μm nodes. In addition, we use these models to design a one-bit pass-gate full adder.

**A. Device and Interconnect Delay**

In this simulation, device delay is evaluated by the inverter delay when both fan-in (FI) and fan-out (FO) equal to one. Interconnect delay is defined as the 50% delay between the starting and ending points of the line driven by minimum size driver, as shown in Fig. 6. Typical lengths are used for local, intermediate, and global copper lines. These lengths are assumed unchanged for different technology nodes.

**Figure 6: Simulation setup to define interconnect delay**

Simulation results are presented in Fig. 7. Data points for 0.25μm nodes come from existing technology. The
trends and values are in good agreement with NTRS projection and published technology data [1, 5].

![Diagram of technology nodes](image)

**Figure 7:** Benchmarked device and interconnect delay

**B. One Bit Full Adder**

A one-bit pass-gate full adder is built and speed tests are been done with our benchmark models. The circuit schematics are shown in Fig. 8. A and B are input bits, C\textsubscript{in} is carry-in bit and C\textsubscript{out} is carry-out bit. At Sum node, a capacitor C\textsubscript{L} is loaded. C\textsubscript{L} is 10\textmu F for 0.18\textmu m technology node and 7\textmu F for 0.13\textmu m. V\textsubscript{dd} is set up to 1.8V and 1.5V for 0.18\textmu m and 0.13\textmu m technology nodes, respectively.

![Circuit schematics of one-bit pass-gate full adder](image)

**Figure 8:** Circuit schematics of one-bit pass-gate full adder

To test the speed of this adder, we switch A from 1 to 0 as B and C\textsubscript{in} stay at 0. The waveforms of A and Sum bits are shown in Fig. 9. t\textsubscript{delay} is the 50\% time delay between them. With devices scaling down from 0.18\mu m to 0.13\mu m, t\textsubscript{delay} is reduced from 0.550ns to 0.375ns. Over 30\% improvement is achieved with scaling.

**Conclusion**

In summary, a convenient customizable predictive BSIM3v3 model has been generated for as low as 70nm L\textsubscript{eff} device and a wide range of interconnect sizes. Extensive evaluations demonstrated the validity of this approach. This predictive technology model could easily be used for early circuit design and research. It is available on the web. Customizable model for the 0.1\mu m node will be available in mid 2000 and 70\mu m node in the following year.

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