NY Times news article:

• Intel will use 3D FinFET for 22nm
• Most radical change in decades
• There is a competing SOI technology
• TSMC, IBM…new transistors soon
• Since 2001 ITRS shows FinFET and ultra-thin-body UTB-SOI as the two successor MOSFETs
• SOITEC UTB-SOI recently available
• IBM 2009 5nm UTB SOI paper
New MOSFET Structures

**FinFET**

**UTBSOI**

**Ultra Thin Body SOI**
Good Old MOSFET Nearing Limits

Vt, S (swing) and Ioff are sensitive to Lg & dopant variations.

- high design cost
- high Vdd, hence high power usage

Finally painful enough for change.

Chenming Hu, July 2011
Power Consumption Problems

1. Not just a chip and package thermal issue.

2. ICs use a few % of world’s electricity today and
   • Power per chip is growing.
   • IC units in use also growing.

3. If power consumption is not reduced, industry future growth is at risk.

Chenming Hu, July 2011
Want Low Vt and Low Ioff

Need smaller S and less variations of S and Vt

Chenming Hu, July 2011
MOSFET becomes “resistor” at very small $L$ --- Drain competes with Gate to control the channel barrier.

How $V_t$ Variation & $S$ Got So Bad

Smaller size or larger $V_d$
Reducing EOT is Not Enough

Gate cannot control the leakage current paths that are far from the gate.

Chenming Hu, July 2011
One of Two Ways to Better $V_t$ and $S$

The gate controls a thin body from more than one side.

FinFET body is a thin fin

N. Lindert et al., DRC paper II.A.6, 2001

Chenming Hu, July 2011
FinFET - 1999

Undoped Body. 30nm etched thin fin. Vt set with gate work-function (SiGe).

X. Huang et al., IEDM, p. 67, 1999

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State-of-the-Art FinFET on Buk Si

20nm Hi Perf
C.C. Wu et al., 2010 IEDM

28nm SoC
C.C. Yeh et al., 2010 IEDM

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FinFET is “Easy” to Scale

because leakage is well suppressed if

Fin thickness =or< Lg

• Thin fin can be made with the same Lg patterning/etching tools.

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Second Way to Better $V_t$ and $S$
Ultra-thin-body SOI (UTB-SOI) $\rightarrow$
No leakage path far from the gate.


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Most Leakage Flows >5nm Below Surface

**Leakage Current Density**

Vgs=0V, Vds=0.7V  
Lg=25nm, Tox=1.5nm


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Silicon Body Needs to be $<Lg/3$

For good swing and device variation


Chenming Hu, July 2011
UTB-SOI

3nm Silicon Body, Raised S/D


Chenming Hu, July 2011
State-of-the-Art 5nm Thin-Body SOI

ETSOI, IBM
K. Cheng et al, IEDM, 2009

Chenming Hu, July 2011
Both Thin-Body Transistors Provide

- Better swing.
- S & Vt less sensitive to Lg and Vd.
- No random dopant fluctuation.
- No impurity scattering.
- Less surface scattering (lower Eeff).

↓

- Higher on-current and lower leakage
- Lower Vdd and power consumption
- Further scaling and lower cost
Back-Gate Bias Option

UTB-SOI

FinFET

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Similarities

• **1996**: UC Berkeley proposed to DARPA two “25nm Transistors”. Both of them
  • use body thickness as a new scaling parameter
  • can use undoped body for high $\mu$ and no RDF

• **1999**: demonstrated FinFET

• **2000**: demonstrated UTB-SOI (Ultra-Thin Body)

• **Since 2001**: ITRS highlights FinFET and UTBSOI

• **Now**: Intel will use Trigate FinFET.
  Soitec readies +-0.5nm substrates for UTBSOI

• **Both FinFET & UTBSOI better than planar bulk!**

Chenming Hu, July 2011
Main Differences

- FinFET body thickness ~ Lg. Investment by fabs
- UTBSOI thickness ~ 1/3 Lg. Investment by Soitec
- FinFET has clear long term scalability. UTBSOI may be ready sooner depending on each firm’s readiness with FinFET.
- FinFET has larger Ion or can use lower Vdd. UTBSOI has a good back-gate bias option.
What May Happen

• FinFET will be used at 22nm by Intel and later by more firms through and beyond 10nm.

• Some firms may use UTBSOI to gain/protect market at 20 or 18nm if FinFET is not option.

  If so, competition between FinFET and UTBSOI will bring out the best of both.

  If not----- back to first bullet.

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BSIM Family Compact Models

Berkeley Short-channel IGFET Models

- BSIM4
- BSIMSOI
- BSIM-MG for FinFETs: in CMC standardization process
- BSIM-IMG for UTB-SOI
FinFET BSIM Compact Model Verified

- FinFET Fabricated at TSMC.
- \( L_g = 30 \text{ nm-10um} \)

\[ \begin{align*}
\text{Drain Current (A)} & \quad \text{Gate Voltage (V)} \\
\text{25 \mu} & \quad 0.0 \quad 0.4 \quad 0.8 \quad 1.2 \\
\text{50 \mu} & \quad 0.0 \quad 0.4 \quad 0.8 \quad 1.2 \\
\end{align*} \]

\[ \begin{align*}
\text{Drain Voltage (V)} & \quad \text{Drain Current (\mu A)} \\
\text{0.0} & \quad 0.0 \quad 0.4 \quad 0.8 \quad 1.2 \\
\text{50} & \quad 0.0 \quad 0.4 \quad 0.8 \quad 1.2 \\
\end{align*} \]

M. Dunga, 2008 VLSI Tech Sym

Chenming Hu, July 2011
Global fitting with 30nm-10um FinFETs

N-Channel MOS
Vds=1.0V
Lg increases

Drain Current (mA)

Gate Voltage (V)

Drain Current (A)

10^-13

10^-10

10^-7

10^-4

0.0 0.2 0.4 0.6 0.8 1.0

0.0 0.2 0.4 0.6 0.8 1.0

0.0 0.2 0.4 0.6 0.8 1.0

0.0 0.2 0.4 0.6 0.8 1.0

Chenming Hu, July 2011
Global fitting with 30nm-10um FinFETs

Transconductance (mA/V) vs. Gate Voltage (V)

N-Channel MOS
Vds=1.0V

Lg increases

Chenming Hu, July 2011
Global fitting with 30nm-10um FinFETs
Temperature Model Verified for FinFET

Drain Current ($\mu$A) vs. Vgs (V)

-50C $\rightarrow$ 200C in steps of 50C
Increasing T

$L_g = 60$nm
20 fins

Drain Current (A) vs. Vgs (V)

-50C $\rightarrow$ 200C in steps of 50C
Increasing T

$L_g = 60$nm
20 fins
Reduce all capacitances.

\[ f \cdot C \cdot V_{dd}^2 \]
Vacuum-Sheath Interconnect

- $C_{\text{TOTAL}} \propto \text{Delay}$, $C_M \propto \text{Crosstalk Noise}$

Load Capacitance: $C_O$
Mutual Capacitance: $C_M$
Total Capacitance: $C_{\text{TOTAL}}$


Chenming Hu, July 2011
Effective $k$ of Vacuum-Sheath Interconnects

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Vacuum Spacer to Reduce $C_{GC}$

- $C_{GOX}$: Gate Oxide Capacitance
- $C_{GC}$: Gate-to-Contact Capacitance

$C_{GOX} \gg C_{GC}$

$C_{GOX} < C_{GC}$

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**Vacuum Spacer Self-Aligned Contact**

20nm MOSFET comparison

<table>
<thead>
<tr>
<th></th>
<th>Oxide Spacer</th>
<th>Vacuum Spacer Self-aligned contact (SAC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter Delay, ps</td>
<td>6.15 (1)</td>
<td>5.05 (0.82)</td>
</tr>
<tr>
<td>Inverter switching energy, fJ</td>
<td>24.2 (1)</td>
<td>18.8 (0.78)</td>
</tr>
<tr>
<td>Relative Area</td>
<td>1</td>
<td>0.7</td>
</tr>
</tbody>
</table>

J. Park, IEEE EDL, p.1368, 2009

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Future Low Voltage Green Transistor

Log Drain Current $I_d$

Gate Voltage $V_g$

$S < 60 \text{mV/dec}$

$S > 60 \text{mV/dec}$

GFET

MOSFET

Chenming Hu, July 2011
How to reduce $V_{dd}$ to 0.15V?

1. Reduce $V_{dd} - V_t$ to < 0.1V with high-mobility-channel material, or sub-threshold circuits.

2. Reduce $V_t$ to 50mV. Need a device that is free of the 60mV/decade turn-off limit.

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Origin of the 60mV/decade Limit

A potential barrier controls the electron flow.

Leakage current is determined by Boltzmann distribution or 60 mV/decade, limiting MOSFET, bipolar, graphene MOSFET...

So, let electrons go **through, not over**, the energy barrier → **semiconductor tunneling** or **MEMS**
Semiconductor Band-to-Band Tunneling: generating electron/hole pairs

A known mechanism of leakage current since 1985.

Called Gate Induce Drain Leakage (GIDL).

J. Chen, P. Ko, C. Hu, IEDM 1985

Chenming Hu, July 2011
Abrupt turn-on due to overlap of valence/conduction bands; adjustable turn-on voltage.
Reduce Vdd by Reducing Eg
Simulated impact of Eg scaling

Vdd scales down faster than Eg.

Eg=0.36eV, Vdd=0.2V, EOT=5 Å, CV/I=0.42pS
Eg=0.69eV, Vdd=0.5V, EOT=7 Å, CV/I=2.2pS
Eg=1.1eV, Vdd=1V, EOT=10 Å, CV/I=4.2pS

Chenming Hu, July 2011
Simulated gFET Inverter VTC

Good voltage gain at 0.1V

Chenming Hu, July 2011

Hetero-junction gFET

• Strained Si on Ge has 0.18eV “effective tunneling Eg”.

• III-V.

A. Bowonder, Intern’l Workshop Junction Tech., 2008

Chenming Hu, July 2011
Summary

- FinFET and UTB-SOI are viable new sub-22nm transistors.
- Different performances, investment costs, wafer costs, scaling barriers.
- Their BSIM SPICE models are available – free 😊
- Capacitance and tunnel gFET are potential opportunities.